

EXHIBIT F

Part 3 of 3



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Doherty et al.

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(54) **PROBE CARD HAVING ON-BOARD
MULTIPLEX CIRCUITRY FOR EXPANDING
TESTER RESOURCES**

(75) Inventors: **C. Patrick Doherty; Jorge L.
deVarona; Salman Akram, all of
Boise, ID (US)**

(73) Assignee: **Micron Technology, Inc., Boise, ID
(US)**

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **09/075,691**

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(51) Int. Cl.⁷ **G01R 31/26**

(52) U.S. Cl. **324/765; 324/754**

(58) Field of Search **324/754, 755,
324/757, 758, 765**

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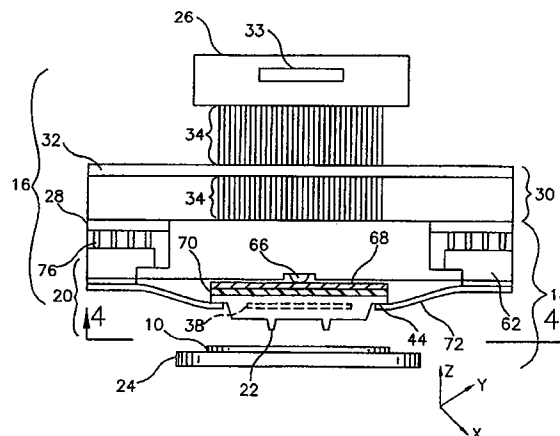
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Primary Examiner—Safet Metjahic
Assistant Examiner—Russell M. Kobert
(74) Attorney, Agent, or Firm—Stephen A. Gratton

(57) **ABSTRACT**

A probe card, a test method and a test system for testing semiconductor wafers are provided. The test system includes the probe card, a tester for generating test signals, and a wafer prober for placing the wafers and probe card in physical contact. The probe card includes contacts for electrically engaging die contacts on the wafer. The probe card also includes an on board multiplex circuit adapted to fan out and selectively transmit test signals from the tester to the probe card contacts. The multiplex circuit expands tester resources by allowing test signals to be written to multiple dice in parallel. Reading of the dice can be performed in groups up to the limit of the tester resources. In addition to expanding tester resources, the multiplex circuit maintains the individuality of each die, and permits defective dice to be electrically disconnected.

19 Claims, 7 Drawing Sheets



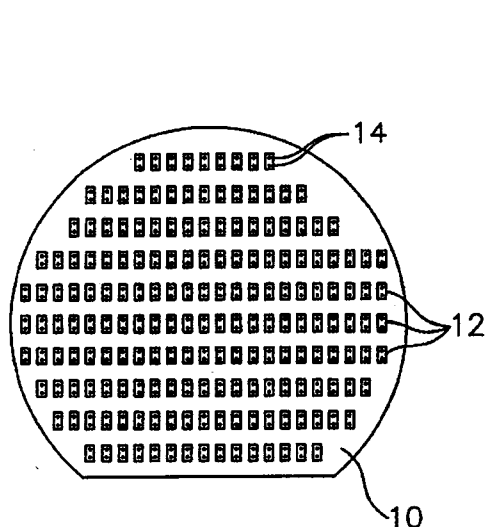
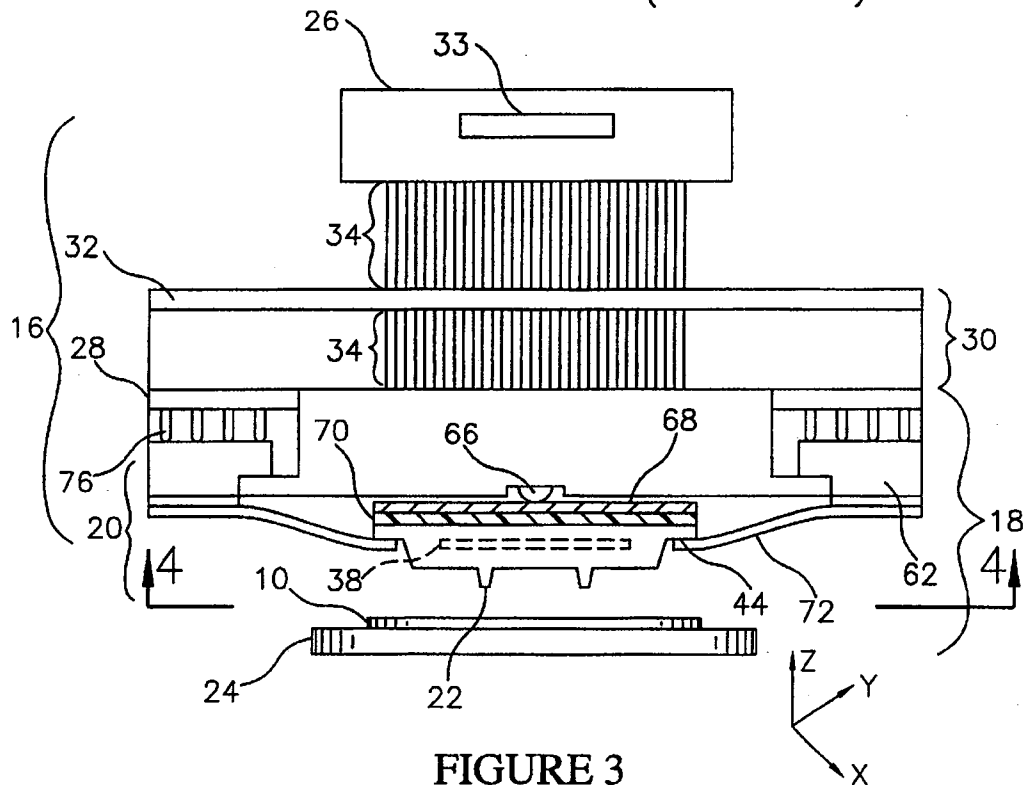


FIGURE 1
(PRIOR ART)

Vcc	1 □	□ 28	Vss
DQ1	2 □	□ 27	DQ8
DQ2	3 □	□ 26	DQ7
DQ3	4 □	□ 25	DQ6
DQ4	5 □	□ 24	DQ5
NC	6 □	□ 23	CAS
WE	7 □	□ 22	OE
RAS	8 □	□ 21	NC
A9	9 □	□ 20	A8
A0	10 □	□ 19	A7
A1	11 □	□ 18	A6
A2	12 □	□ 17	A5
A3	13 □	□ 16	A4
Vcc	14 □	□ 15	Vss

FIGURE 2
(PRIOR ART)



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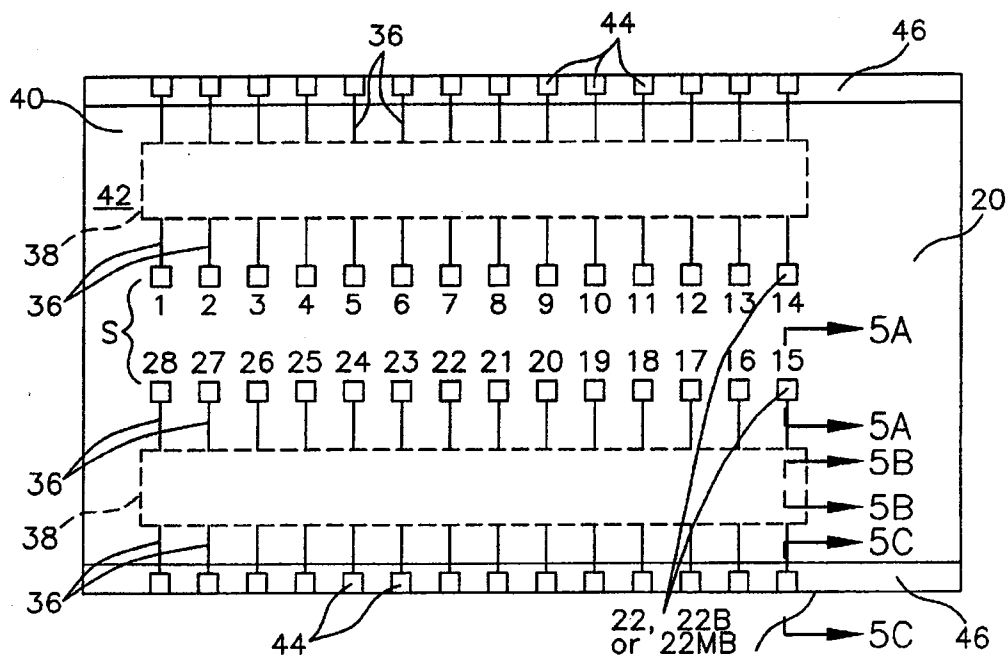


FIGURE 4

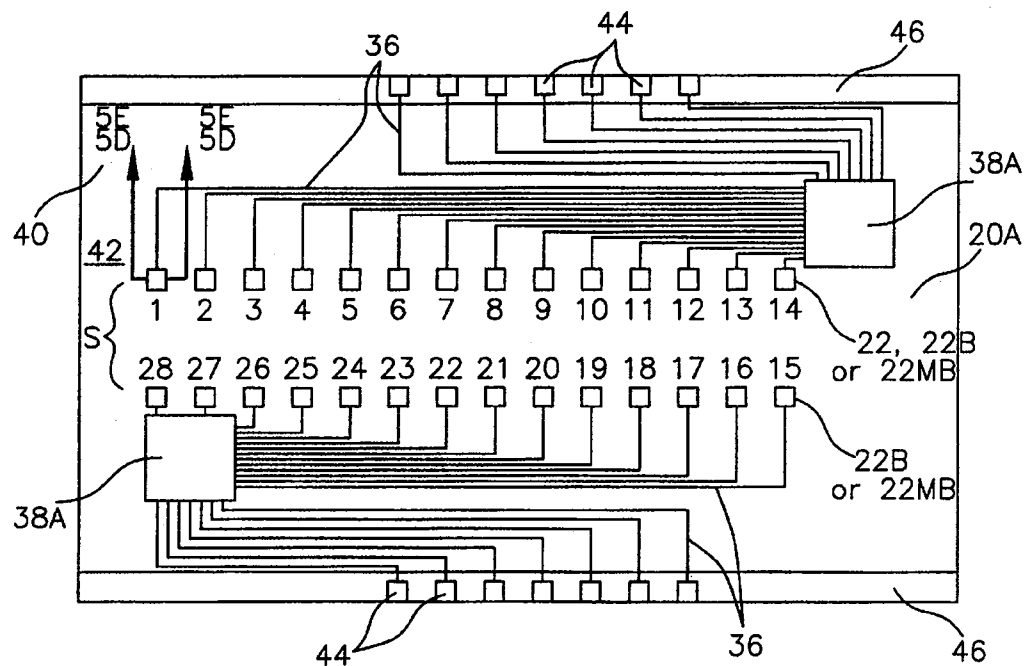


FIGURE 4A

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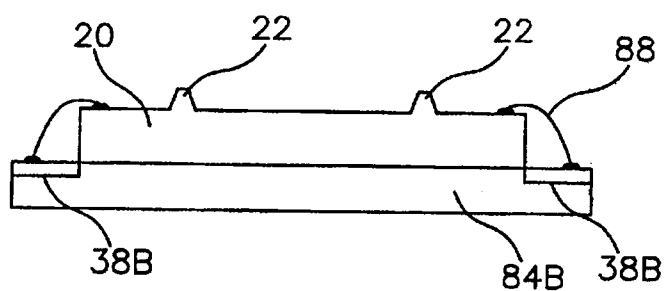


FIGURE 4B

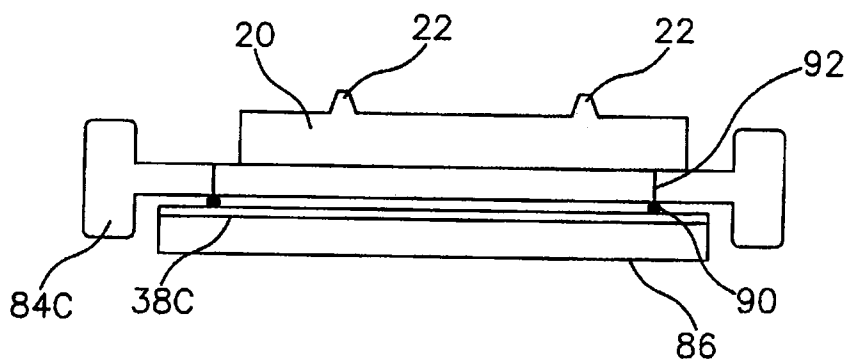


FIGURE 4C

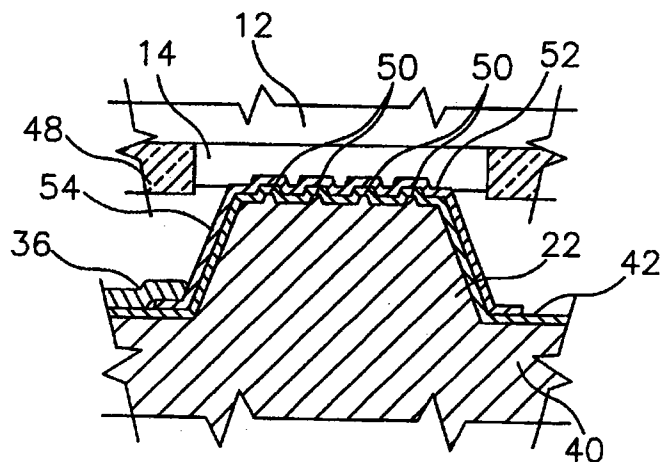


FIGURE 5A

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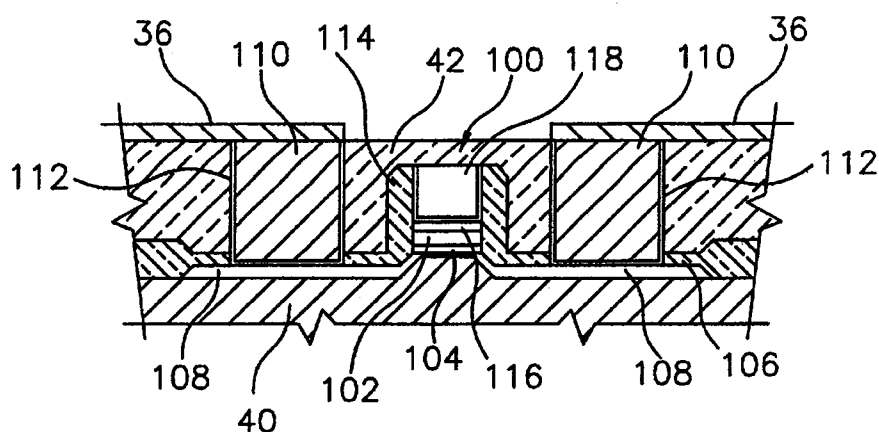


FIGURE 5B

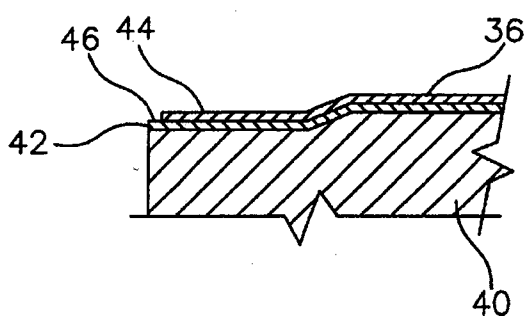


FIGURE 5C

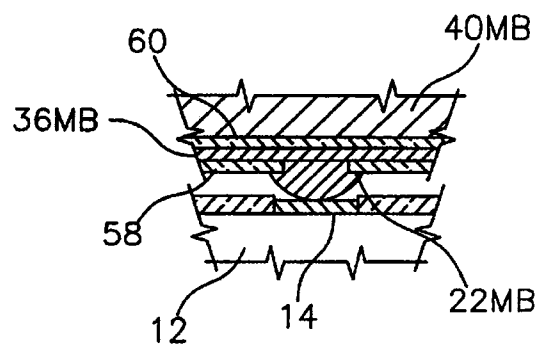


FIGURE 5D

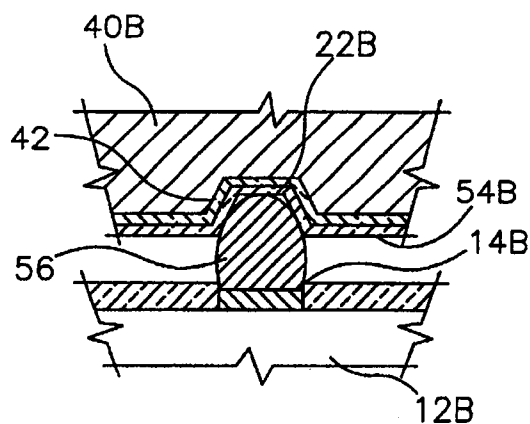


FIGURE 5E

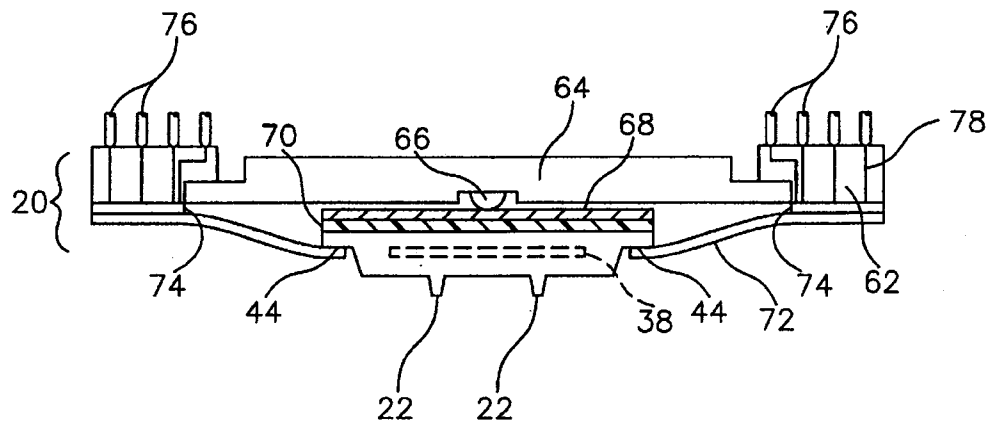


FIGURE 6

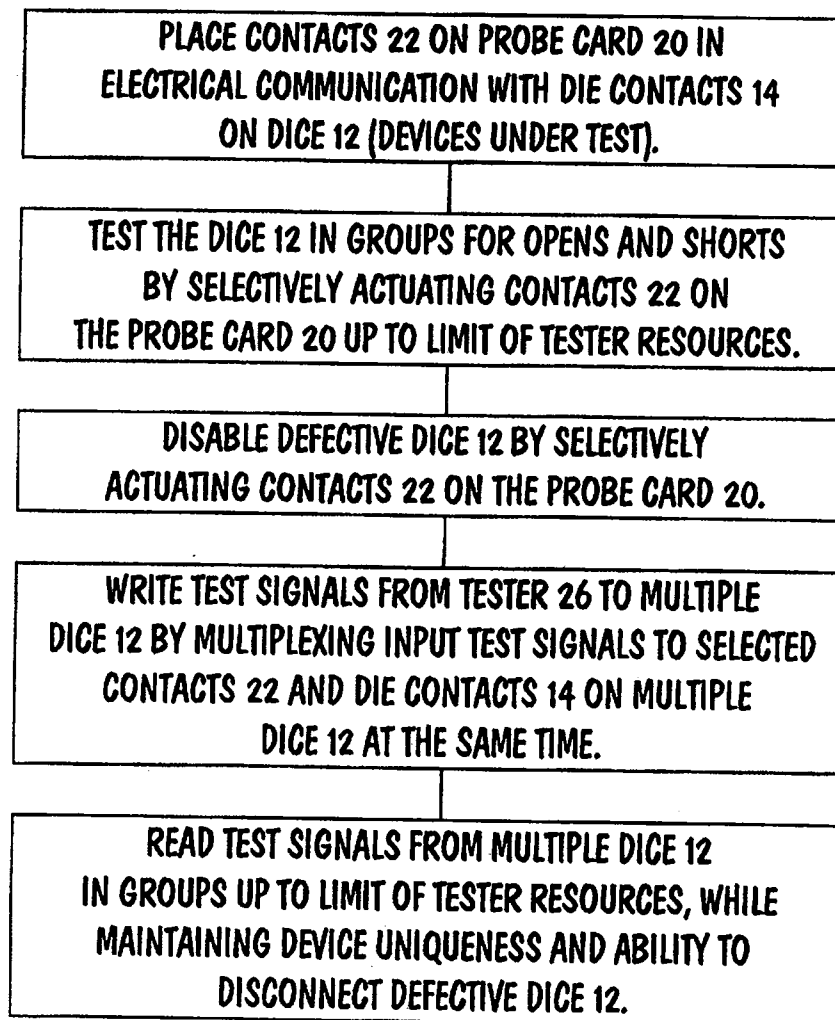


FIGURE 7

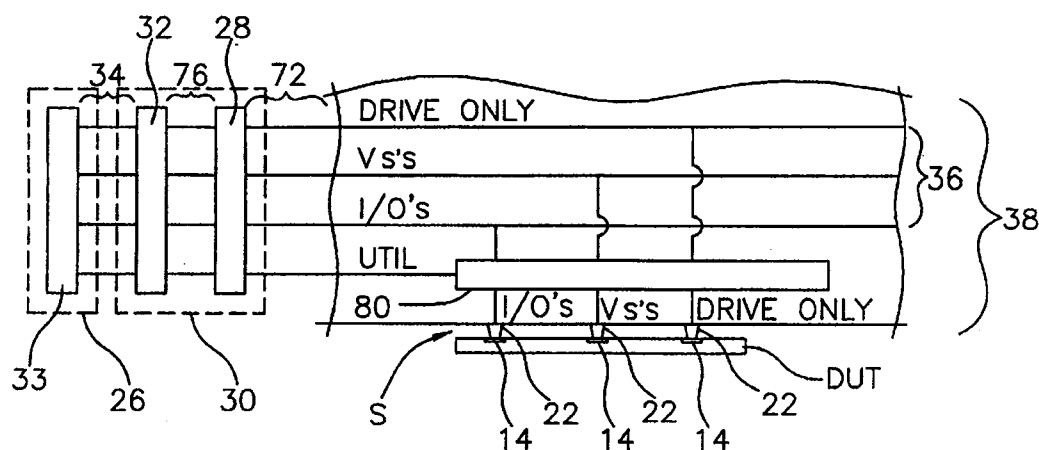


FIGURE 8A

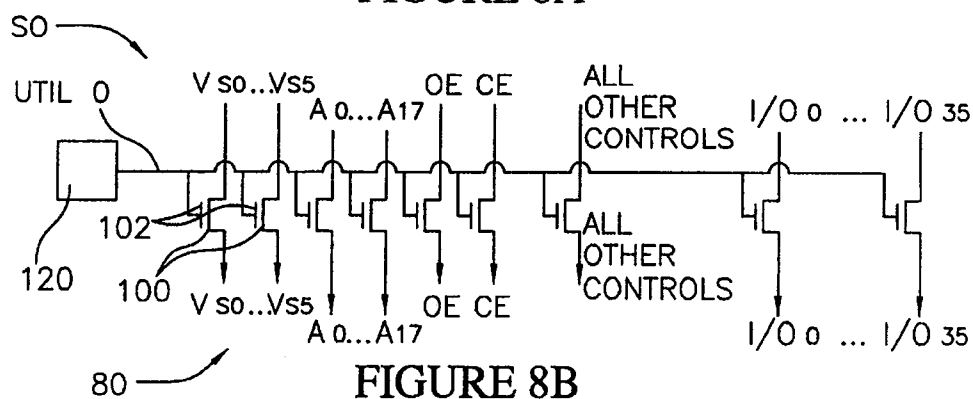
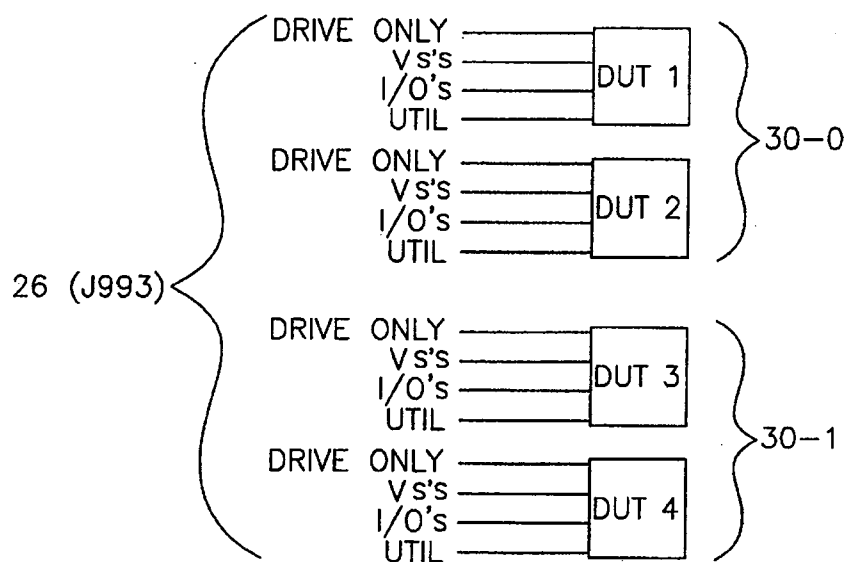


FIGURE 8B

FIGURE 8C
(PRIOR ART)

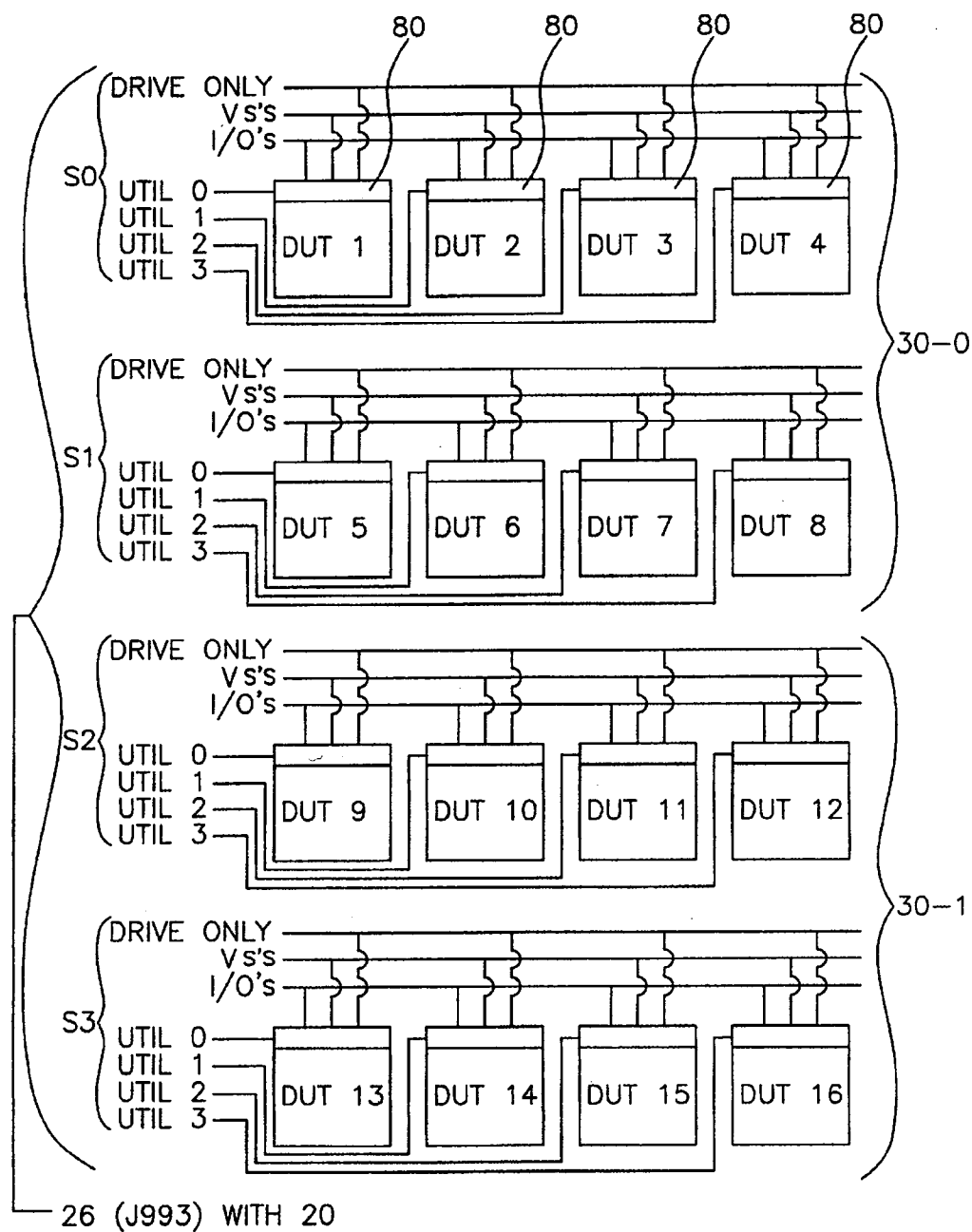


FIGURE 8D

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PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES

FIELD OF THE INVENTION

This invention relates generally to semiconductor manufacture and specifically to a probe card for testing semiconductor wafers. This invention also relates to test systems and test methods employing the probe card.

BACKGROUND OF THE INVENTION

Semiconductor wafers are tested prior to singulation into individual die, to assess the electrical characteristics of the integrated circuits contained on each die. A typical wafer-level test system includes a wafer prober for handling and positioning the wafers, a tester for generating test signals, a probe card for making temporary electrical connections with the wafer, and a prober interface board to route signals from the tester pin electronics to the probe card.

The test signals can include specific combinations of voltages and currents transmitted through the pin electronics channels of the tester to the probe interface board, to the probe card, and then to one or more devices under test on the wafer. During the test procedure response signals such as voltage, current and frequency can be analyzed and compared by the tester to required values. The integrated circuits that do not meet specification can be marked or mapped in software. Following testing, defective circuits can be repaired by actuating fuses to inactivate the defective circuitry and substitute redundant circuitry.

Different types of probe cards have been developed for probe testing semiconductor wafers. The most common type of probe card includes elongated needle probes configured to electrically engage die contacts, such as bond pads, or other contacts on the wafer. An exemplary probe card having needle probes is described in U.S. Pat. No. 4,563,640 to Hasegawa et al.

Although widely used, needle probe cards are difficult to maintain and unsuitable for high parallelism applications, in which multiple dice must be tested at the same time. In addition, needle probe cards are not suitable for some applications in which the dice have high count die contact requirements, such as bond pads in dense grid arrays. In particular, the long needles and variations in the needles lengths makes it difficult to apply a constant gram force to each die contact. Long needles can also generate parasitic signals at high speeds (e.g., >500 MHZ).

A similar type of probe card includes buckle beams adapted to flex upon contact with the wafer. This type of probe card is described in U.S. Pat. No. 4,027,935 to Byrnes et al. Although better for high count die contacts, and high parallelism applications, buckle beam probe cards are expensive, and difficult to maintain.

Another type of probe card, referred to as a "membrane probe card", includes a membrane formed of a thin and flexible dielectric material such as polyimide. An exemplary membrane probe card is described in U.S. Pat. No. 4,918,383 to Huff et al. With membrane probe cards, contact bumps are formed on the membrane in electrical communication with conductive traces, typically formed of copper.

One disadvantage of membrane contact bumps is that large vertical "overdrive" forces are required to penetrate oxide layers and make a reliable electrical connection with the die contacts on the dice. These forces can damage the die contacts and the dice. In addition, membrane probe cards

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can be repeatedly stressed by the forces, causing the membrane to lose its resiliency. Use of high probe temperatures can also cause the membrane to lose resiliency.

Another disadvantage of membrane probe cards is the CTE (coefficient of thermal expansion) mismatch between the membrane probe card and wafer. In the future, with decreasing size of each die contact, higher parallelism requirements, and increased probing temperatures, maintaining electrical contact with the die contacts will be increasingly more difficult. In addition, because of relatively large differences between the CTE of membrane probe cards and silicon wafers, maintaining electrical contact between a large number of dice and a membrane probe card will be almost impossible.

Yet another limitation of conventional test systems, and a disadvantage of conventional probe cards, is that full functionality testing must be performed at the die level rather than at the wafer level. These tests require a large number of connections with the dice, and separate input/output paths between the dice and test circuitry. For functional test procedures on dice having multiple inputs and outputs, an input/output path must be provided to several die contacts at the same time. The number of dice that can be tested in parallel is always limited by the number of drive only, and input/output channels the tester provides, as well as the die contact arrangements on the dice. The number of drive only and input/output channels is fixed for a particular test system by its manufacturer.

To maintain speed characteristics for high count die contacts, the die contacts must be distributed throughout, or around the edges of the dice in a dense array. With this arrangement it is very difficult to parallel probe multiple dice using needle type probe cards, and impossible with dice having high count die contacts. Buckle beam probe cards are a costly alternative for probing dice having high count die contacts.

In view of the foregoing, improved probe cards capable of testing wafers with large numbers of dice, and high count die contacts, at high speeds, are needed in the art. In addition, probe cards capable of expanding tester resources to accommodate high parallelism, and high count die contact testing applications are needed in the art.

SUMMARY OF THE INVENTION

In accordance with the present invention, a probe card, a test system, and a test method for testing semiconductor dice contained on a wafer are provided. The probe card is adapted for use with a conventional tester and wafer prober. The probe card includes an on board multiplex circuit adapted to fan out, and selectively transmit, test signals from the tester to the wafer in response to control signals. The multiplex circuit includes active electrical switching devices, such as FETs, operable by control signals generated by a controller.

The multiplex circuit allows tester resources to be fanned out to multiple devices under test, while maintaining the uniqueness of each device, and the ability to disconnect failing devices. The additional control of the test signals also speeds up the testing process, and allows higher wafer throughputs using the same tester resources.

In addition to the multiplex circuit, the probe card includes a substrate, and a pattern of contacts formed on the substrate. During a test procedure, the probe card contacts make temporary electrical connections with die contacts on the wafer. Each probe card contact can be enabled or disabled as required by the multiplex circuit, to selectively write (send) the test signals to the die contacts, and to selectively read (receive) output signals from the die contacts.

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The probe card and its contacts can be configured to electrically engage one die at a time, or multiple dice at the same time, up to all of the dice contained on the wafer. In an exemplary test procedure, dice can be tested for opens and shorts in groups corresponding to the available tester resources. Next, multiple dice can be written to in parallel by multiplexing drive only and I/O resources of the tester. Following the write step, multiple dice can be read in parallel in groups corresponding to the available tester drive only and I/O resources.

With the probe card comprising a semiconducting material such as silicon, the multiplex circuit can include integrated circuits and active electrical switching devices, formed directly on the substrate, using semiconductor circuit fabrication techniques. Alternately, the multiplex circuit can be fabricated on an interposer mounted to the probe card substrate, or on a die attached to the probe card substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a prior art semiconductor wafer containing multiple semiconductor dice;

FIG. 2 is a plan view of a prior art semiconductor die illustrating die contacts on a face of the die and exemplary Ad functional designations for the die contacts;

FIG. 3 is a schematic cross sectional view of a test system constructed in accordance with the invention;

FIG. 4 is an enlarged plan view taken along section line 4—4 of FIG. 3 illustrating a probe card constructed in accordance with the invention;

FIG. 4A is an enlarged plan view equivalent to FIG. 4 of an alternate embodiment probe card;

FIG. 4B is a schematic cross sectional view of another alternate embodiment probe card;

FIG. 4C is a schematic cross sectional view of another alternate embodiment probe card;

FIG. 5A is an enlarged cross sectional view taken along section line 5A—5A of FIG. 4, following contact of the probe card and wafer, and illustrating probe card contacts electrically engaging die contacts on the wafer;

FIG. 5B is an enlarged cross sectional view taken along section line 5B—5B of FIG. 4, illustrating a FET transistor of on board circuitry contained on the probe card;

FIG. 5C is an enlarged cross sectional view taken along section line 5C—5C of FIG. 4 illustrating a bonding pad on the probe card;

FIG. 5E is an enlarged cross sectional view taken along section line 5E—5E of FIG. 4A illustrating an alternate embodiment probe card contact electrically engaging a bumped die contact on the wafer;

FIG. 5D is an enlarged cross sectional view taken along section line 5D—5D of FIG. 4A illustrating an alternate embodiment probe card contact electrically engaging a die contact on the wafer;

FIG. 6 is an enlarged view of a portion of FIG. 3 illustrating the probe card;

FIG. 7 is a block diagram illustrating steps in a method for testing in accordance with the invention;

FIG. 8A is a schematic electrical diagram of on board circuitry and a test site contained on the probe card and the electrical interface of the probe card and tester;

FIG. 8B is a schematic electrical diagram of a multiplex circuit of the on board circuitry;

FIG. 8C is a schematic electrical diagram illustrating a test operation for a tester with a prior art probe card; and

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FIG. 8D is a schematic electrical diagram illustrating a test operation for the tester of FIG. 8C but with a probe card and multiplex circuit constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a prior art semiconductor wafer 10 includes multiple semiconductor dice 12 fabricated using processes that are well known in the art. As shown in FIG. 2, each die 12 includes multiple die contacts 14 formed thereon. The die contacts 14 comprise metal pads in electrical communication with integrated circuits contained on the die 12.

Following singulation of the wafer 10, the dice 12 can be packaged. In this case, the die contacts 14 can be wire bonded to lead fingers formed on a leadframe. The singulated dice 12 can also be used in unpackaged form as known good die (KGD). In this case, the die contacts 14 can be wire bonded to a substrate, such as a printed circuit board, or alternately flip chip mounted using reflowed solder bumps. The singulated dice 12 can also be included in chip scale packages. In this case, interconnects such as conductive bumps electrically contact the die contacts 14 to establish electrical communication with external contacts on a substrate.

For illustrative purposes, each die 12 includes twenty eight die contacts 14 with the functional designations indicated in FIG. 2. However, as is apparent, the number and functional arrangements of the die contacts 14 are merely exemplary, and other arrangements are possible.

Referring to FIG. 3, a test system 16 constructed in accordance with the invention, and configured to test the dice 12 contained on the wafer 10. The test system 16 includes a test head 30 and a probe card 20. The probe card 20 includes probe card contacts 22 configured to make temporary electrical connections with the die contacts 14. The test system 16 also includes a wafer prober 18 wherein the probe card 20 is mounted, and a tester 26 configured to apply test signals through the probe card 20, to the dice 12 contained on the wafer 10, and to analyze the resultant signals. The wafer prober 18 includes a probe card holder 62 for mounting and electrically interfacing with the probe card 20. Further details of the mounting of the probe card 20 to the test head 30 will be hereinafter described.

The wafer prober 18 includes a wafer chuck 24 configured to move in X and Y directions to align the wafer 10 with the probe card 20, and in the Z direction to move the wafer 10 into contact with the probe card 20. One suitable wafer prober 18 is manufactured by Electroglass and is designated a Model 4080.

The test system 16 also includes a prober interface board 28 for routing test signals from the test head 30 to the probe card 20. In addition, the prober interface board 28 can be in electrical communication with tester pin electronics 32 in the test head 30. The tester pin electronics 32 provide separate electrical paths 34 from test circuitry 33 contained in the tester 26, to the test head 30 and to the prober interface board 28.

The signal generating and analyzing capability of the test circuitry 33, and the number of separate electrical paths 34 provided by the tester pin electronics 32, are termed herein as "tester resources". In general, the configurations of the test circuitry 33, and of the electrical paths 34, are fixed for a particular tester 26 by the manufacturer. For example, the test circuitry 33 can be configured to route drive only signals

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through some of the electrical paths 34, and input/output channels through other of the electrical paths 34, as required for testing a particular type of die 12. Exemplary testers 26 are commercially available from Teradyne of Boston MA, as well as other manufacturers.

Referring to FIG. 4, further details of the probe card 20 are illustrated. The contacts 22 on the probe card 20 are arranged in patterns corresponding to the patterns of the die contacts 14. Each pattern of contacts 22 represents a single test site (S). For simplicity, only one pattern of contacts 22 and one test site (S) on the probe card 20 is illustrated. However, in actual practice, the probe card 20 can include multiple patterns of contacts 22 forming multiple test sites (S1 . . . Sn) to accommodate testing of multiple dice 12 at the same time. The contacts 22 on the test site S are designated 1-28 in correspondence with the die contacts 14 (FIG. 2).

In order to test multiple dice 12 at the same time certain conditions must be met. Firstly, the patterns of contacts 22 must exactly match the patterns of the die contacts 14. In addition, the stepping distance (i.e., x-y repeat and pattern spacing) must be the same for the contacts 22 as for the die contacts 14. Secondly, the software that controls the stepping process must be able to pick valid test sites. For example, when testing at the edges of a round wafer with a probe card that includes rectangular or square patterns of contacts 22, some patterns of contacts 22 will not have an associated device under test. It is also desirable to not have contacts 22 contacting a passivation layer 48 (FIG. 5A) on the dice 12 as this can damage the contacts 22.

In general, the use of the probe card 20 can greatly reduce the number of steps necessary for the prober 18 to test all of the dice 12 contained on the wafer 10. In the extreme case, rather than using stepping methods, the probe card 20 can be formed with enough patterns of contacts 22 to simultaneously contact every die contact 14 for all of the dice 12 on the wafer 10. Test signals can then be selectively applied and electronically switched as required, to selected dice 12 on the wafer 10. The probe card 20 can be formed with any desired number of test sites (S1 . . . Sn). In addition, the probe card 20 can be configured to test a complete semiconductor wafer 10, or to test a portion of the dice 12 in a partial wafer, or other substrate.

Still referring to FIG. 4, in addition to the patterns of contacts 22, the probe card 20 includes patterns of conductors 36 in electrical communication with the contacts 22 and with on-board circuitry 38. The contacts 22 and conductors 36 are formed on a substrate 40 of the probe card 20.

In the embodiment illustrated in FIG. 5A, the substrate 40 comprises silicon (or another semiconducting material such as gallium arsenide). This permits the on-board circuitry 38 to be formed as integrated circuits on the substrate 40 using semiconductor circuit fabrication techniques such as doping, CVD, photolithography, and etching. Also, with the substrate 40 comprising silicon, a coefficient of thermal expansion of the probe card 20 exactly matches that of the wafer 10. The substrate 40 can also comprise a silicon containing material, such as silicon-on-glass, and the on board circuitry can be formed on a layer of the substrate 40.

Preferably, the substrate 40 is thick enough to resist deflection and buckling during test procedures using the probe card 20. In addition, an electrically insulating layer 42, such as SiO₂, polyimide, or BPSG can be formed on the substrate 40 to provide insulation for the contacts 22 and conductors 36 from the bulk of the substrate 40.

The conductors 36 on the substrate 40 are in electrical communication with the probe card contacts 22, and with the

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on board circuitry 38. The conductors 36 can be formed on a surface of the substrate 40 in a required pattern. In addition, the conductors 36 can include interlevel segments, such as metal vias or other interlevel electrical paths, that are in electrical communication with other components of the on-board circuitry 38.

In addition, the conductors 36 can be placed in electrical communication with the test circuitry 33 to provide electrical paths from the test circuitry 33 (FIG. 3) to the on-board circuitry 38, and to the contacts 22. Preferably, the conductors 36 comprise a highly conductive metal such as copper, aluminum, titanium, tantalum, tungsten, molybdenum or alloys of these metals. The conductors 36 can be formed as a single layer of metal, or as a multi metal stack, using a thin film metallization process (e.g., CVD, patterning, etching). Alternately, a thick film metallization process (e.g., screen printing, stenciling) can be used to form the conductors 36.

The conductors 36 also include bonding pads 44 located along the peripheral edges of the probe card 20. The bonding pads 44 provide bonding sites for forming separate electrical paths from the probe card holder 62 (FIG. 1) to each of the conductors 36. Preferably the bonding pads 44 are located on recessed surfaces 46 (FIG. 5C) along the edges of the substrate 40 to provide clearance for TAB bonds, wire bonds, spring loaded connectors (e.g., "POGO PINS") or other electrical connections to the bonding pads 44.

Referring to FIG. 5A, the probe card contacts 22 are shown in an enlarged cross sectional view. In the embodiment of FIG. 5A, the contacts 22 comprise raised members that project from a surface of the substrate 40. The raised contacts 22 help to provide a separation distance between the probe card 20 and the wafer 10 to clear any particulate contaminants that may be present on the opposing surfaces. In addition, the contacts 22 can include penetrating projections 50 adapted to penetrate the die contacts 14 to a limited penetration depth. To limit the penetration depth, the penetrating projections 50 have a height that is less than a thickness of the die contacts 14. For thin film aluminum die contacts 14, this thickness will typically be less than about 1.0 μm . As also shown in FIG. 5A, surfaces 52 at the tips of the contacts 22 provide stop planes for limiting penetration of the contacts 22 into the die contacts 14. These stop plane surfaces 52 along with the dimensions of the penetrating projections 50 insures that the contacts 22 minimally damage the die contacts 14 during a test procedure.

The contacts 22 and penetrating projections 50 can be formed integrally with the substrate 40 using a bulk micro-machining process. With such a process, an etch mask (e.g., Si₃N₄ layer) can be formed on the substrate 40 and a suitable etchant, such as KOH, can be used to etch the substrate 40 to form the contacts 22. Solid areas of the etch mask determine the peripheral dimensions and shape of the contacts 22. The etch rate and time of the etch process determine the etch depth and the height of the contacts 22. Such a process permits the contacts 22, and penetrating projections 50, to be formed accurately, and in a dense array to accommodate testing of dense arrays of die contacts 14.

A representative height of the contacts 22 can be from 50 μm to 100 μm . A representative width of the contacts 22 on a side can be from 25 μm to 80 μm . A spacing of the contacts 22 matches the spacing of the die contacts 14. A height of the penetrating projections 50 can be from about 2000 Å-5000 Å.

Still referring to FIG. 5A, each contact 22 is covered with a conductive layer 54 in electrical communication with a conductor 36. The conductive layers 54 for all of the

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contacts 22 can be formed of a metal layer deposited and patterned to cover the contacts 22, or other selected areas of the substrate 40. By way of example, the conductive layers 54 for the contacts 22 can comprise aluminum, copper, titanium, tungsten, tantalum, platinum, molybdenum, cobalt, nickel, gold, iridium or alloys of these metals. Some of these materials such as gold and platinum are non-reactive so that material transfer between the contacts 22 and the die contacts 14 can be minimized. The conductive layers 54 can also comprise a metal silicide or a conductive material such as doped polysilicon. Further, the conductive layers 54 can comprise a bi-metal stack including a base layer, and a non-reactive and oxidation resistant outer layer, such as gold or platinum.

The conductive layers 54 can be formed using a metallization process that includes blanket deposition (e.g., CVD), formation of a resist mask, and then etching. Preferably, the resist mask comprises a thick film resist that can be deposited to a thickness greater than a conventional resist. One suitable resist is a negative tone, thick film resist sold by Shell Chemical under the trademark "EPON RESIN SU-8".

The conductive layer 54 for each contact 22 is in electrical communication with a corresponding conductor 36 formed on the substrate 40. The conductive layers 54 and conductors 36 can be formed at the same time using the same metallization process. Alternately, the conductors 36 can be formed of a different metal than the conductive layers 54 using separate metallization process.

A process for fabricating the contacts 22 on a silicon substrate, substantially as shown in FIG. 5A is described in U.S. Pat. No. 5,483,741, entitled "METHOD FOR FABRICATING A SELF LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMICONDUCTOR DICE", and in U.S. Pat. No. 5,686,317 entitled "METHOD FOR FORMING AN INTERCONNECT HAVING A PENETRATION LIMITED CONTACT STRUCTURE FOR ESTABLISHING A TEMPORARY ELECTRICAL CONNECTION WITH A SEMICONDUCTOR DIE", both of which are incorporated herein by reference.

Referring to FIG. 5B, an enlarged cross sectional view of a FET transistor 100 of the on board circuitry 38 is illustrated. As is apparent the FET transistor 100 is merely one component of the on board circuitry 38. The on board circuitry 38 can include many FET transistors 100, as well as additional components, to provide the circuit arrangements that will be hereinafter explained. Further, other active electrical switching devices, such as NPN or PNP transistors can be used in place of the FET transistor 100 illustrated in the preferred embodiment.

The FET transistors 100 can be formed integrally with the substrate 40 using semiconductor circuit fabrication techniques. A suitable process sequence can include initially etching the contacts 22 (FIG. 5A) and penetrating projections 50 (FIG. 5A) and then fabricating the FET transistors 100. Following formation of the FET transistors 100, the insulating layer 42 can be formed, the conductive layers 54 (FIG. 5A) can be formed, and the conductors 36 can be formed. Each FET transistor 100 includes a polysilicon gate 102, and a gate oxide 104. In addition, a field oxide 106 is formed on the substrate 40 for electrically isolating the FET transistors 100. The substrate 40 also includes N+ active areas 108, which can be formed by implanting dopants into the substrate 40 to form the sources and drains of the FET transistors 100. Metal filled vias 110 with metal silicide layers 112, electrically connect the sources and drains of the FET transistors 100 to the conductors 36. The FET transis-

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tors 100 also include spacers 114, TEOS layers 116 and nitride caps 118.

Referring to FIG. 4A, an alternate embodiment probe card 20A is illustrated. The probe card 20A is substantially similar to the probe card 20 previously described, but includes on board circuitry 38A formed on a surface of the substrate 40 rather than being formed integrally therewith. For example, the on board circuitry 38A can be included in a separate die mounted to the substrate 40, and then interconnected to the conductors 36. In this case the die containing the on board circuitry can be wire bonded or flip chip mounted to the substrate 40 in electrical communication with the contacts 14. In this embodiment the substrate 40 can comprise silicon, ceramic, or a glass filled resin (FR-4).

As another alternative, the on board circuitry can be included on an interposer attached to the probe card 20. Examples of interposers are shown in FIGS. 4B and 4C. In FIG. 4B, an interposer 84B includes on-board circuitry 38B, substantially as previously described. The interposer 84B can comprise a semiconducting material such as silicon, in which case the on-board circuitry 38B can be fabricated on the interposer 84B using semiconductor circuit fabrication techniques. Wire 88 can then be bonded to pads on the probe card 20 and to pads on the interposer 84A to provide separate electrical paths there between.

Alternately, as shown in FIG. 4C, on-board circuitry 38C can be contained on a die 86 attached to an interposer 84C (or directly to the probe card 20). In the embodiment of FIG. 4C, the die 86 is flip chip mounted to the interposer 84C. Reflowed solder bumps 90 on the die 86 are bonded to internal conductors 92 on the interposer 84C. In addition, the internal conductors 92 are in electrical communication with the contacts 22 on the probe card 20.

Referring to FIG. 5D, the probe card 20A can include contacts 22MB which are attached to the substrate 40 rather than being formed integrally therewith. As shown in FIG. 5D, the probe card contacts 22MB comprise metal microbumps formed on a polymer film 58 similar to multi layered TAB tape. In addition, conductors 36MB are formed on an opposing side of the polymer film 58 in electrical communication with the contacts 22MB. A compliant adhesive layer 60 attaches the polymer film 58 to a substrate 40MB. Further details of contact 22MB are described in U.S. Pat. No. 5,678,301, entitled "METHOD FOR FORMING AN INTERCONNECT FOR TESTING UNPACKAGED SEMICONDUCTOR DICE".

Another alternate embodiment probe card contact 22B is illustrated in FIG. 5E. Contacts 22B are configured to electrically engage die contacts 14B having solder bumps 56 formed thereon. The contacts 22B permit a bumped die 12B to be tested. The contacts 22B comprise indentations formed in a substrate 40B. In this embodiment the substrate can comprise silicon, gallium arsenide, ceramic or other substrate material. The indentations can be etched or machined to a required size and shape and then covered with conductive layers 54B. The contacts 22B are configured to retain the solder bumps 56. In addition, the conductive layers 54B for the contacts 22B are in electrical communication with conductors equivalent to the conductors 36 previously described. Further details of contact 22B are described in U.S. Pat. No. 5,962,921, entitled "INTERCONNECT HAVING RECESSED CONTACT MEMBERS WITH PENETRATING BLADES FOR TESTING SEMICONDUCTOR DICE AND PACKAGES WITH CONTACT BUMPS", incorporated herein by reference.

Referring to FIG. 6, further details of the test system 16 and probe card 20 are illustrated. The wafer prober 18

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includes the probe card holder 62, a force applying fixture 64 and a force applying mechanism 66. These items can be components of a conventional wafer prober as previously described. The force applying mechanism 66 presses against a pressure plate 68 and a compressible member 70 to bias the probe card 20 against the wafer 10. By way of example, the compressible member 70 can be formed of an elastomeric material such as silicone, butyl rubber, or fluorosilicone; in foam, gel, solid or molded configurations.

In addition, a flexible membrane 72 is bonded to the probe card 20 and to the probe card holder 62. In general, the flexible membrane 72 functions to physically attach the probe card 20 to the probe card holder 62. In addition, the flexible membrane 72 functions to provide electrical paths between the contacts 22 and the test circuitry 33 (FIG. 3) of the tester 26. The flexible membrane 72 can be formed of thin flexible materials to allow movement of the probe card 20 in Z-directions. For example, the flexible membrane 72 can be formed of a flexible multi layered material similar to TAB tape.

In the illustrative embodiment, the flexible membrane 72 comprises a layer of polymer tape having metal conductors thereon. Bonded connections are formed between the conductors on the membrane 72 and corresponding conductors 74 on the probe card holder 62. In addition, bonded connections are formed between the conductors on the membrane 72 and the bonding pads 44 on the probe card 20.

Still referring to FIG. 6, the wafer prober 18 includes spring loaded electrical connectors 76 which are in electrical communication with the prober interface board 28. One type of spring loaded electrical connector 76 is manufactured by Pogo Industries of Kansas City, Mo. under the trademark "POGO PINS". The electrical connectors 76 electrically communicate with internal conductors 78 on the probe card holder 62.

The probe card mounting arrangement shown in FIG. 6, as well as others, are described in U.S. Pat. No. 6,060,891, entitled "PROBE CARD FOR SEMICONDUCTOR WAFERS AND METHOD AND SYSTEM FOR TESTING WAFERS", incorporated herein by reference. However, it is to be understood that these mounting arrangements are merely exemplary and the probe card 20 can be mounted in a conventional manner on a commercially available wafer prober.

TEST METHOD

Referring to FIG. 7, steps in a method for testing the wafer 10 using the test system 18 and probe card 20 are illustrated. These steps are as follows.

1. Place contacts 22 on probe card 20 in electrical communication with die contacts 14 on dice 12 (devices under test).

2. Test the dice 12 in groups for opens and shorts by selectively actuating contacts 22 on the probe card 20 up to limit of tester resources.

3. Disable defective dice 12 by selectively actuating contacts 22 on the probe card 20.

4. Write test signals from tester 26 to multiple dice 12 by multiplexing input test signals to selected contacts 22 and die contacts 14 on multiple dice 12 at the same time.

5. Read test signals from multiple dice 12 in groups up to limit of tester resources, while maintaining device uniqueness and ability to disconnect defective dice 12.

Multiplex Circuit

Referring to FIGS. 8A-8D, further details of the on board circuitry 38 (FIG. 4A) are illustrated. In FIG. 8A a single test

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site S is illustrated. The test site S on the probe card 20 includes a pattern of contacts 22 which are configured to electrically engage die contacts 14 on a device under test DUT. As previously described, the probe card 20 is in electrical communication with the probe card holder 62, the tester pin electronics 32, and the test circuitry 33 within the tester 26.

As shown in FIG. 8A, the on board circuitry 38 includes a multiplex circuit 80. The multiplex circuit 80 is configured to receive test signals from the test circuitry 33 and to fan out or multiply the test signals. In addition, the multiplex circuit 80 is configured to selectively address the fanned out test signals through the probe card contacts 22 to selected die contacts 14 on the DUT. Stated differently, the multiplex circuit permits the test signals to be fanned out, allowing test procedures to be conducted in parallel. At the same time, the multiplex circuit 80 is configured to maintain the uniqueness of individual DUTs, and to electrically disconnect defective DUTs as required.

As shown in FIG. 8A, the multiplex circuit 80 includes a Util channel for each DUT, which functions as a control channel. In addition to the Util channel, the multiplex circuit 80 includes drive only channels, Vs channels, and I/O channels. The numbers of the channels are determined by the tester resources. Table I lists the tester resources of a model "J993" tester 26 manufactured by Teradyne.

TABLE I

Tester Resources of Teradyne "J993" Tester	
16 power supply channels per test head (30)	
16X, 16Y address generation channels per test head (30)	
16 DUTs can be tested in parallel per test head (30)	
72 I/O channels per test head (30)	
2 heads (30) per tester (26)	
320 drive only channels per head (30) divisible as follows:	
80 per test site (S) with 4 test sites (S0-S3)	
40 per test site (S) with 8 test sites (S-S7)	
20 per test site (S) with 16 test sites (S0-S15)	
Up to 320 megabits of catch RAM	
36 Util channels per test head (30)	

Table II lists the tester resources of a model "J994" tester 26 manufactured by Teradyne.

TABLE II

Tester Resources of Teradyne "J994" Tester	
32 power supply channels per test head (30)	
16X, 16Y address generation channels per test head (30)	
32 DUTs can be tested in parallel per test head (30)	
144 I/O channels per test head (30)	
2 heads (30) per tester (26)	
640 drive only channels per head 30 divisible as follows:	
80 per test site (S) with 8 test sites (S1-S8)	
40 per test site (S) with 16 test sites (S1-S16)	
20 per test site (S) with 32 test sites (S1-S32)	
Up to 640 megabits of catch RAM	
52 Util channels per test head (30)	

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Table III lists the test requirements for one type of SRAM.

TABLE III

Sample SRAM Requirements For Each Device Under Test DUT	
36 I/O channels per DUT	
18 address channels (drive only) per DUT	
32 control channels (drive only) per DUT	
6 power supply channels (Vs-voltage supplies) per DUT	
Util channels used depends on parallelism	
Total	
36 I/O channels per DUT	
50 drive only channels per DUT	
6 Vs channels per DUT	

With these sample requirements a "J993" tester 26 can test two DUTs per test head 30, due to the I/O requirements. This is shown schematically in FIG. 8C. In FIG. 8C, the (J993) tester 26 includes a first test head 30-0 and a second test head 30-1. Each test head 30-0, 30-1, is capable of testing two DUTs, for a total of four at a time. Following testing of these four DUTs, both wafers 10 (one on each test head) can be stepped such that four additional DUTs align with the probe card contacts for testing.

A "J994" tester 26 has twice the tester resources of a "J993" tester 26. Accordingly on the basis of the above sample I/O requirements, a "J994" tester 26 can test four DUTs per test head 30, for a total of eight at a time.

Referring to FIG. 8B, a single test site S of the multiplex circuit 80 is illustrated. The multiplex circuit 80, simply stated, comprises multiple FET transistors 100 configured to provide a switching circuit for selectively enabling and disabling the contacts 22 on the probe card 20. The gate 102 of each FET transistor 100 is in electrical communication with the Util 0 channel. A controller 120 (or computer) generates control signals which are transmitted through the Util 0 channel to the FET transistors 100.

In the illustrative embodiment the multiplex circuit 80 is configured to test the SRAM of Table III. Accordingly, there are six Vs channels (Vs0 . . . Vs5), eighteen address channels (A0 . . . A17), and thirty six I/O channels (I/O0-I/O35). In addition, there is an OE channel, a CE channel, and an "all other controls" channel. With this arrangement test signals can be transmitted from the test circuitry 33 and latched by the channels. Control signals from the controller 120 then control the FET transistors 100 to enable and disable the contacts 22 to selectively transmit the test signals to the die contacts 14 as required.

During the test mode the uniqueness of each DUT is maintained. In addition, the control signals can be used operate the FET transistors 100 to disable selected contacts 22 in order to electrically disconnect defective DUTs. Still further, the control signals can be used to operate the FET transistors 100 to enable and disable selected contacts 22 in the transmission of "read" signals from the DUTs. However, in the "read" mode the DUTs must be read in accordance with the tester resources.

As is apparent, the multiplex circuit 80 illustrated in FIG. 8B is merely exemplary. Those skilled in the art, with the aid of the present specification, can design other multiplex circuits able to multiply and selectively address test signals from a tester. Thus other types of multiplexing circuits are intended to be included within the scope of the present claims.

Referring to FIG. 8D, the operation of the J993 tester 26 of Table I, outfitted with the probe card 20 having the multiplex circuit 80 is illustrated. In this example there are four test sites S0, S1, S2, S4 contained in two test heads

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30-0, 30-1. Using the multiplex circuit each test site can write test signals to four DUTs at a time. In the "read" mode the additional three DUTs per test site must be selected in accordance with tester resources (e.g., one at a time or two at a time).

A limiting factor in the number of DUTs that can be tested by each test site is the drive current capacity of the channels of the tester 26. On the J993 and J994 testers 26, the drive current capacity is about 50 mA per channel. In addition, the test signals can be specified with a current (IOL) of about 8 mA per channel. Thus with some margin, each I/O channel and drive only channel of the tester 26 can be configured to drive four DUTs substantially as shown in FIG. 8D. During a write operation there is 8 mA per DUT×4 DUTs=32 mA per tester drive only channel. This leaves a 18mA per channel margin.

Thus the invention provides an improved probe card for testing semiconductors wafers, a method for testing semiconductor wafers using the probe card, and a test system employing the probe card. The probe card can include contacts in dense arrays to accommodate testing of multiple dice having dense arrays of die contacts. In addition, the probe card includes on board circuitry configured to expand tester resources.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A probe card for testing a semiconductor wafer having a plurality of wafer contacts comprising:

a substrate comprising a semiconductor material;

a plurality of contacts on the substrate configured to make temporary electrical connections with the wafer contacts, the contacts comprising raised portions of the substrate, projections on the raised portions for penetrating the wafer contacts, and conductive layers on the projections for electrically contacting the wafer contacts; and

a multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices in electrical communication with the contacts, the circuit configured to fan out test signals from a tester, and to control the contacts to selectively transmit the test signals to the wafer contacts.

2. The probe card of claim 1 wherein the semiconductor material comprises silicon.

3. A probe card for testing a semiconductor wafer having a plurality of wafer contacts comprising:

a substrate comprising a semiconductor material;

a plurality of contacts on the substrate configured to make temporary electrical connections with the wafer contacts; and

a multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices on the substrate in electrical communication with the contacts, and configured to fan out test signals from a tester, the multiplex circuit operable in response to control signals to selectively enable and disable the contacts to permit selective transmission of the test signals to the wafer contacts.

4. The probe card of claim 3 wherein the semiconductor material comprises silicon and the contacts comprise etched portions of the substrate.

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5. The probe card of claim 3 wherein the contacts comprise a plurality of projections for penetrating the wafer contacts.

6. The probe card of claim 3 wherein the contacts comprise a plurality of test sites, with each of the test sites configured to test a device under test on the wafer.

7. In a test system including a tester for generating test signals, a probe card for applying the test signals to a semiconductor wafer having a plurality of wafer contacts comprising:

a substrate comprising a semiconductor material;

a plurality of contacts comprising raised portions of the substrate and penetrating projections on the raised portions at least partially covered by conductive layers configured to electrically contact the wafer contacts; and

a multiplex circuit comprising a plurality of integrated circuits integral with the substrate in electrical communication with the contacts, the multiplex circuit configured to fan out the test signals to expand resources of the tester;

the integrated circuits comprising a plurality of active electrical switching devices, each of the devices in electrical communication with a contact and operable by control signals to selectively enable and disable the contact, to allow the test signals to be selectively transmitted to a selected wafer contact.

8. The probe card of claim 7 wherein the contacts comprise etched portions of the substrate.

9. The probe card of claim 7 wherein the raised portions comprise surfaces configured to limit a penetration depth of the projections into the wafer contacts.

10. A test system for a semiconductor wafer having a plurality of wafer contacts comprising:

a tester comprising test circuitry for generating test signals and a plurality of electrical paths in electrical communication with the test circuitry, the tester having tester resources determined by a signal generating and analyzing capability and by a number of the electrical paths;

a probe card comprising a substrate comprising a semiconductor material;

a plurality of contacts comprising portions of the substrate at least partially covered with conductive layers configured to make temporary electrical connections with the wafer contacts; and

a multiplex circuit comprising integrated circuits integral with the substrate including a plurality of active electrical switching devices in electrical communication with the tester and with the contacts, the multiplex circuit configured to expand the tester resources by fanning out at least some of the test signals to the contacts while allowing a defective device under test to be electrically disconnected.

11. The probe card of claim 10 wherein the test signals include write signals and the multiplex circuit is configured to fan out and transmit the write signals to a plurality of devices under test on the wafer.

12. The probe card of claim 10 wherein the semiconductor material comprises silicon and the contacts comprise etched portions of the substrate.

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13. A test system for testing a semiconductor wafer having a plurality of wafer contacts comprising:

a tester configured to transmit test signals to the wafer, the tester comprising test circuitry for generating test signals and a plurality of electrical paths in electrical communication with the test circuitry, the tester having tester resources determined by a signal generating and analyzing capability and by a number of the electrical paths;

a probe card comprising a substrate comprising a semiconductor material;

a plurality of contacts on the substrate in electrical communication with the electrical paths configured to electrically contact the wafer contacts; and

a multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices in electrical communication with the contacts, the circuit configured to fan out the test signals from the tester, and to control the contacts to selectively transmit the test signals to the wafer contacts for expanding the tester resources.

14. The test system of claim 13 wherein the contacts comprise projections for penetrating the wafer contacts.

15. The test system of claim 13 wherein the contacts are at least partially covered with conductive layers.

16. The test system of claim 13 wherein the contacts comprise etched portions of the substrate with projections configured to penetrate the second contacts.

17. A test system for testing a semiconductor wafer having a plurality of wafer contacts comprising:

a tester comprising test circuitry and a plurality of electrical paths configured to transmit write test signals to the wafer and to analyze read test signals from the wafer, the tester having tester resources determined by the test circuitry and the electrical paths;

a probe card comprising a semiconductor substrate and a plurality of contacts on the substrate comprising portions of the substrate at least partially covered by conductive layers in electrical communication with the electrical paths and configured to electrically contact the wafer contacts;

a multiplex circuit on the probe card in electrical communication with the contacts and configured to multiply the test signals for expanding the tester resources; the multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices, each of the devices in electrical communication with a contact on the probe card and operable by control signals to selectively enable and disable the contact, to allow the test signals to be selectively transmitted to a selected wafer contact.

18. The test system of claim 17 wherein the semiconductor material comprises silicon and the contacts comprise etched portions of the substrate.

19. The test system of claim 17 further comprising a wafer prober and a flexible membrane physically and electrically attaching the probe card to the wafer prober.

* * * * *



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(54) **TEST PARALLELISM INCREASE BY
TESTER CONTROLLABLE SWITCHING OF
CHIP SELECT GROUPS**

Publication Classification(51) **Int. Cl.****G11C 29/00**

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(52) **U.S. Cl. 365/201**

(76) **Inventors:** Norbert Rehm, Apex, NC (US); Rath
Ung, Apex, NC (US); Rob Perry, Cary,
NC (US); Jan Zieleman, Cary, NC
(US); Dirk Fuhrmann, Apex, NC (US)

(57)

ABSTRACT

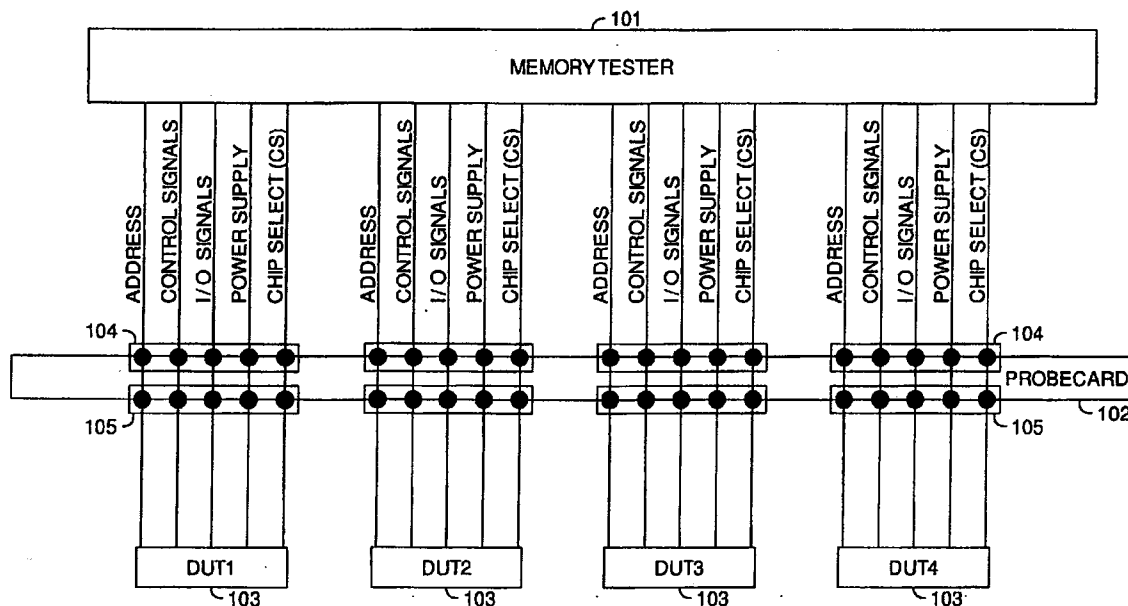
Correspondence Address:

PATTERSON & SHERIDAN, LLP
Gero McClellan / Infineon / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056 (US)

Embodiments of the invention generally provide methods and systems for increasing the level of parallelism in testing memory devices. A set of test signals provided by a memory tester may be shared by two or more devices under test. A chip selector may be used to select at least one or all the devices sharing a given set of test signals. By sharing test signals between multiple devices, the level of parallel testing may be increased without increasing the pin count and complexity of memory testers and probe cards.

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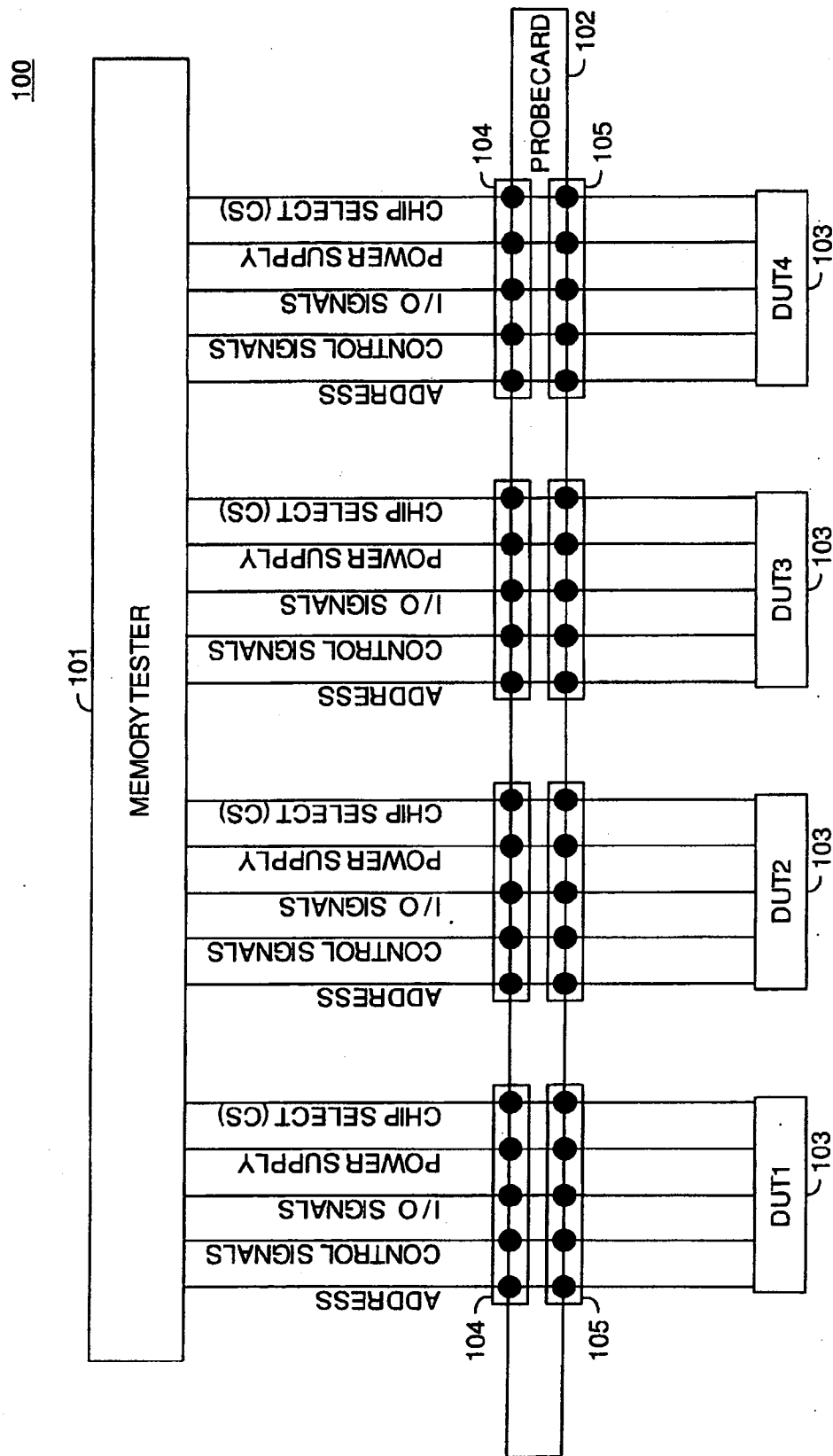


FIG. 1

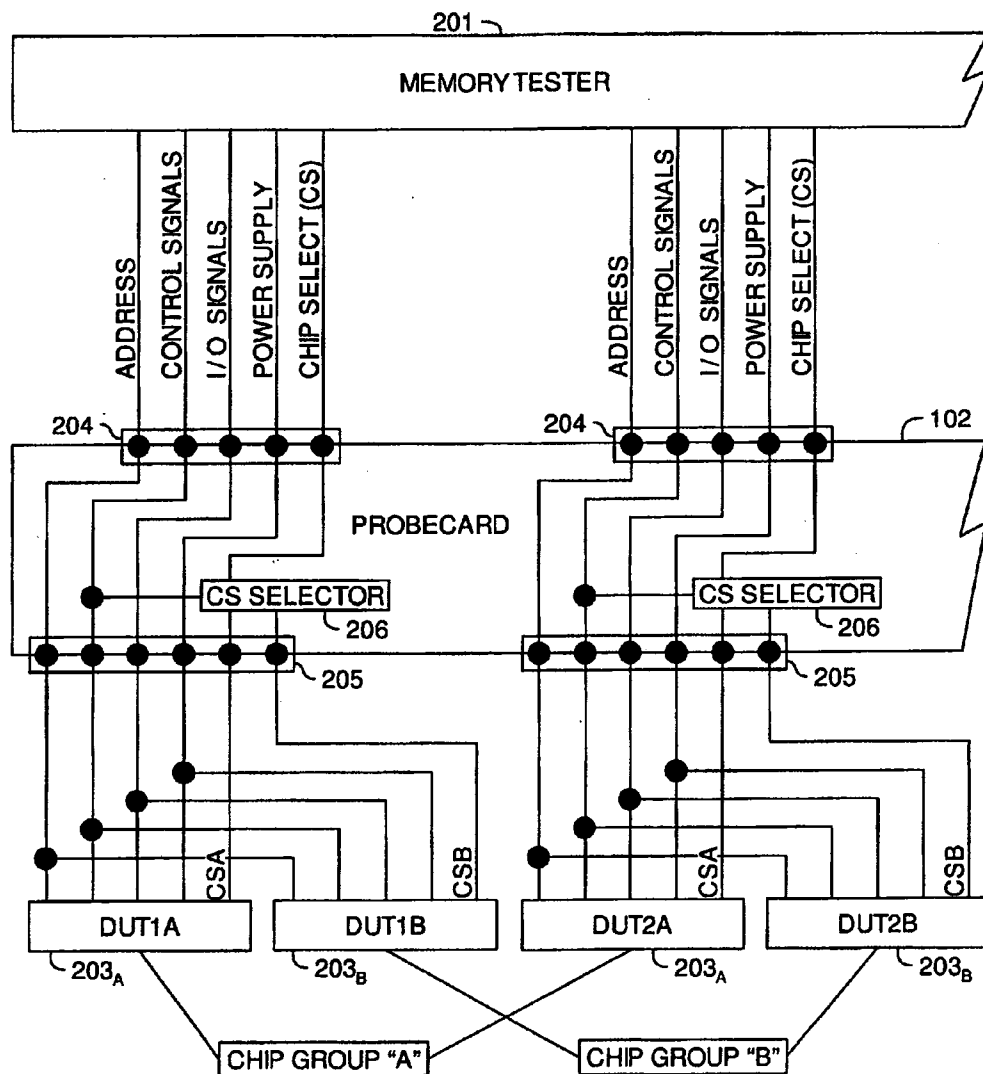
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FIG. 2A

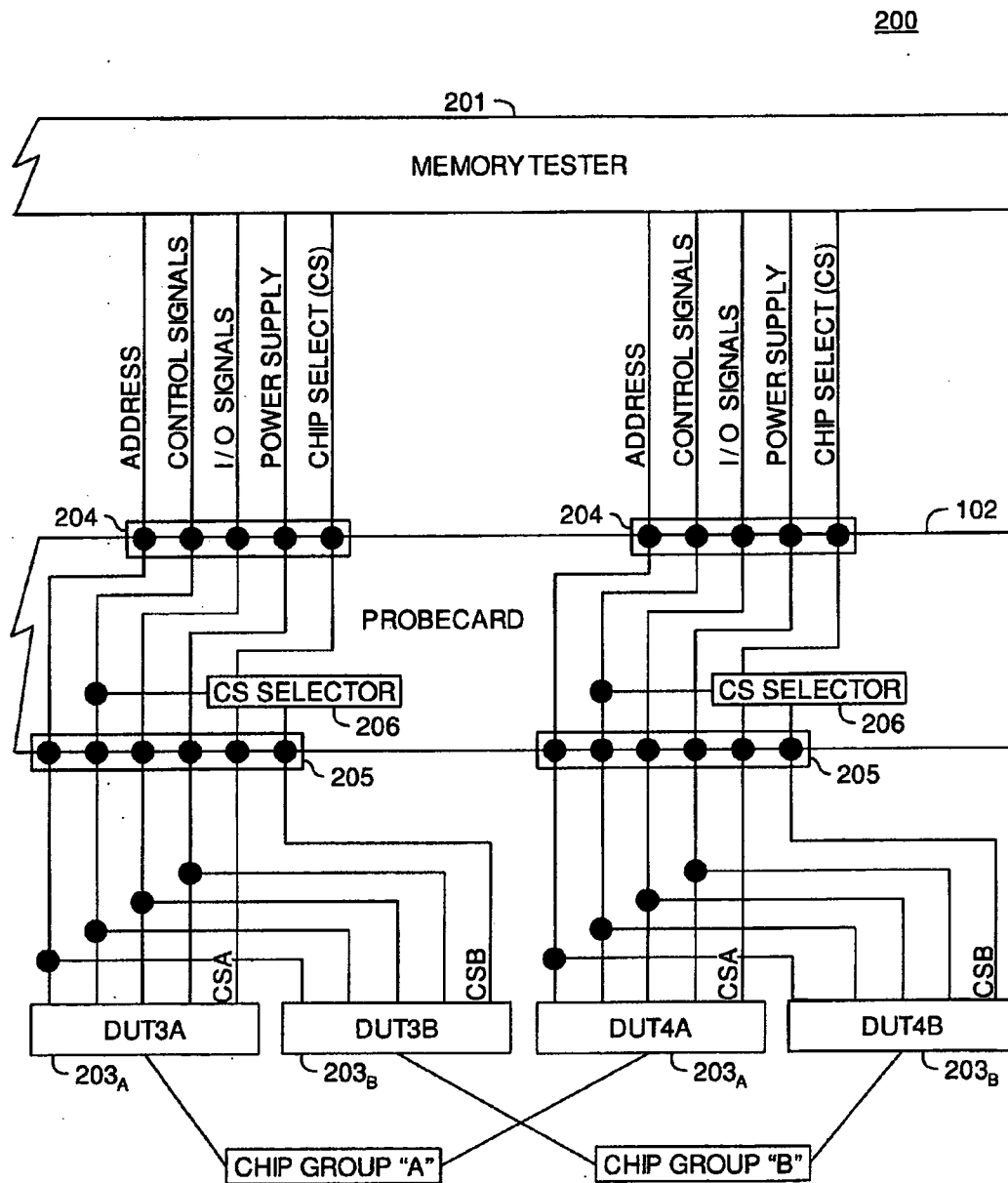


FIG. 2B

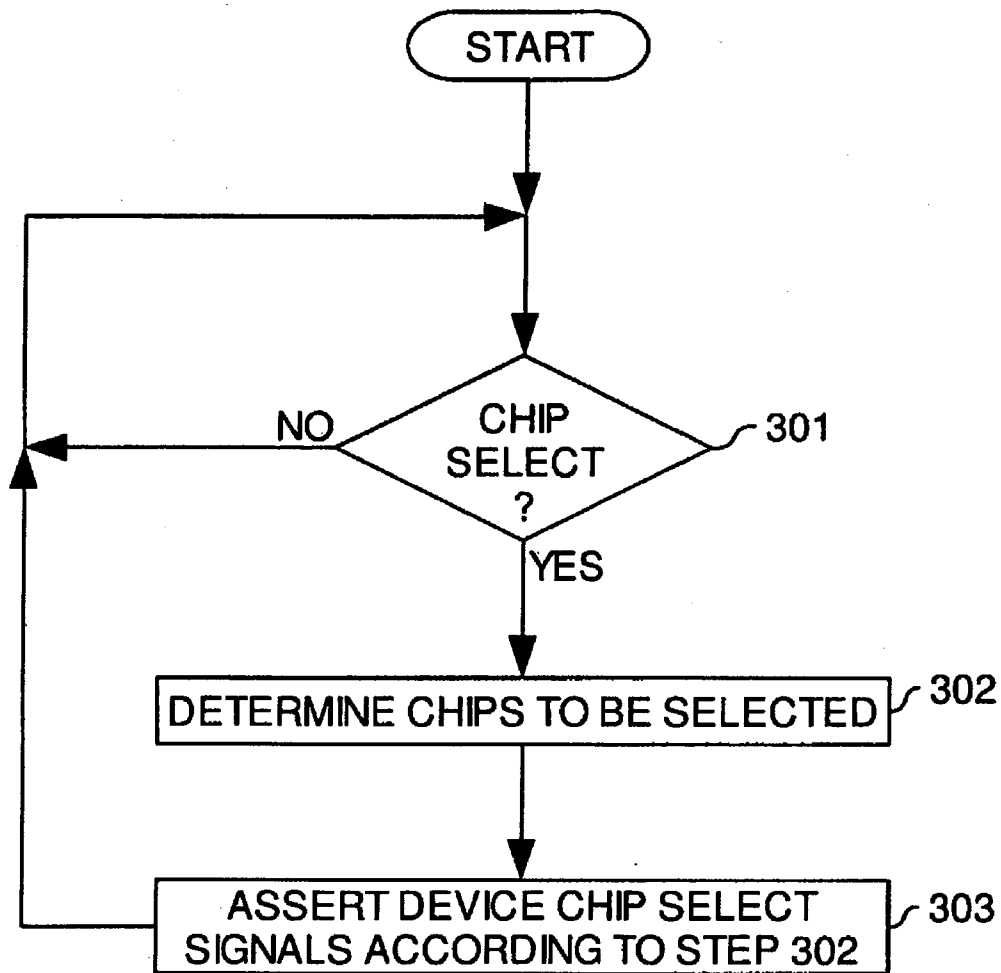


FIG. 3

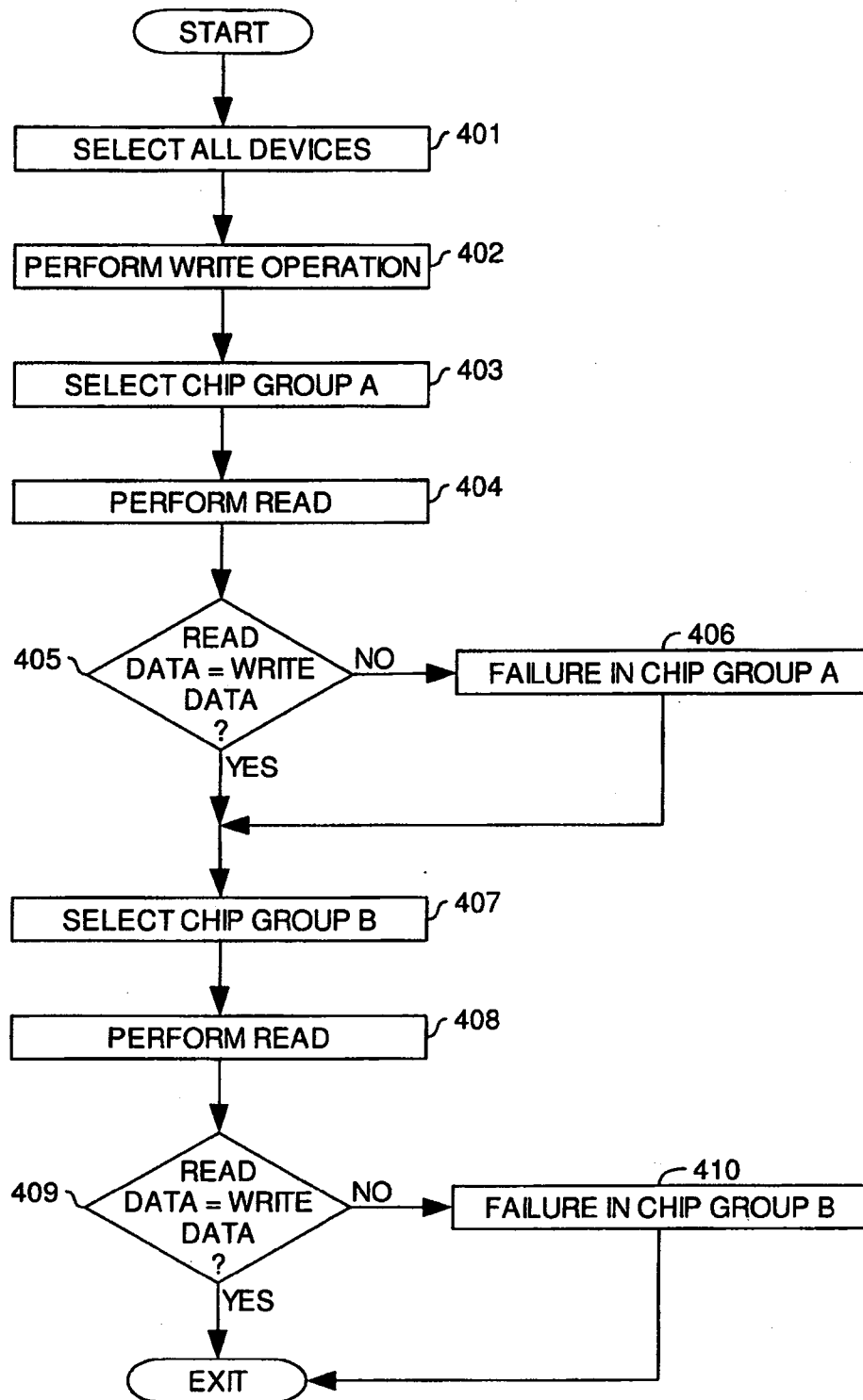
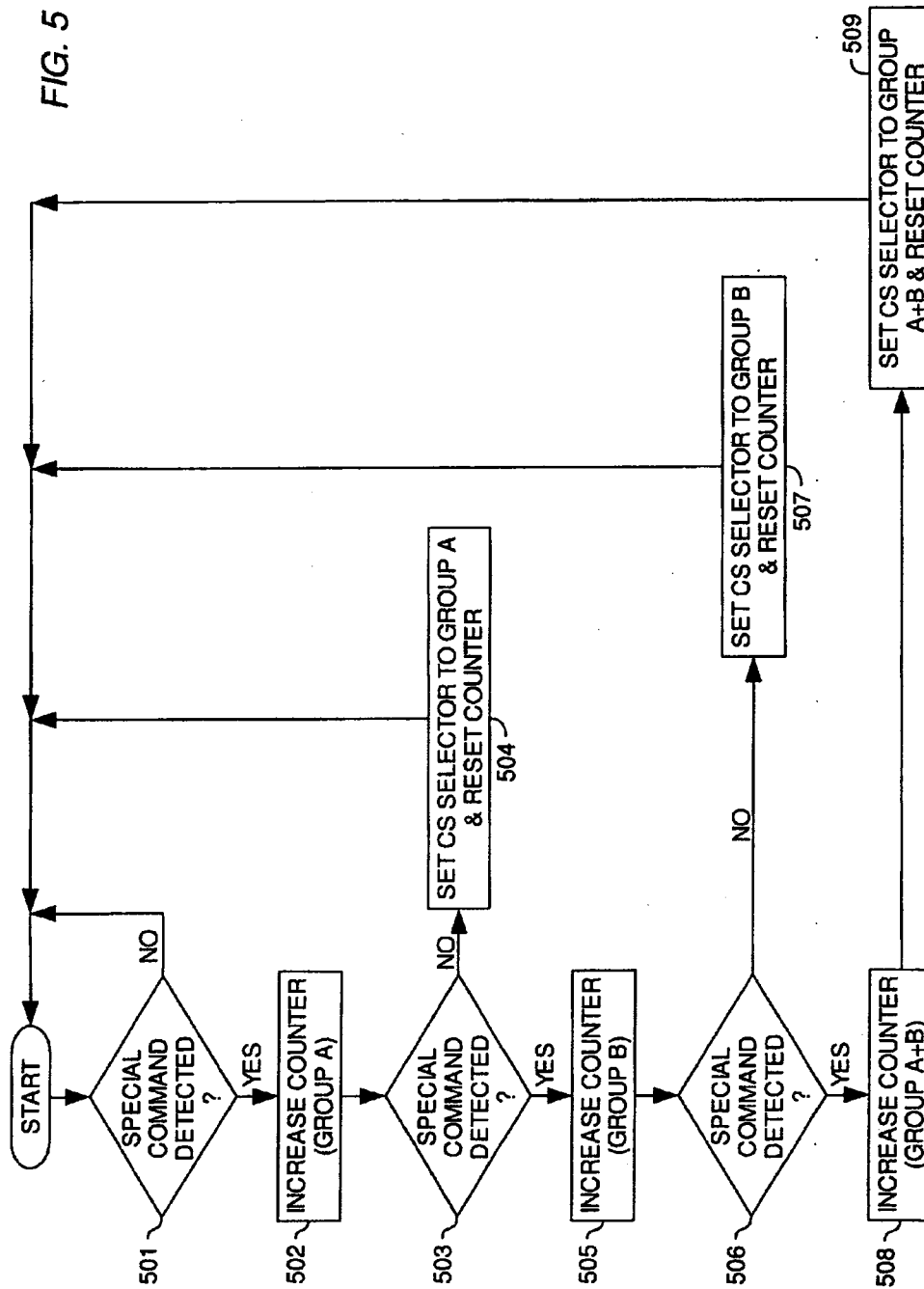


FIG. 4



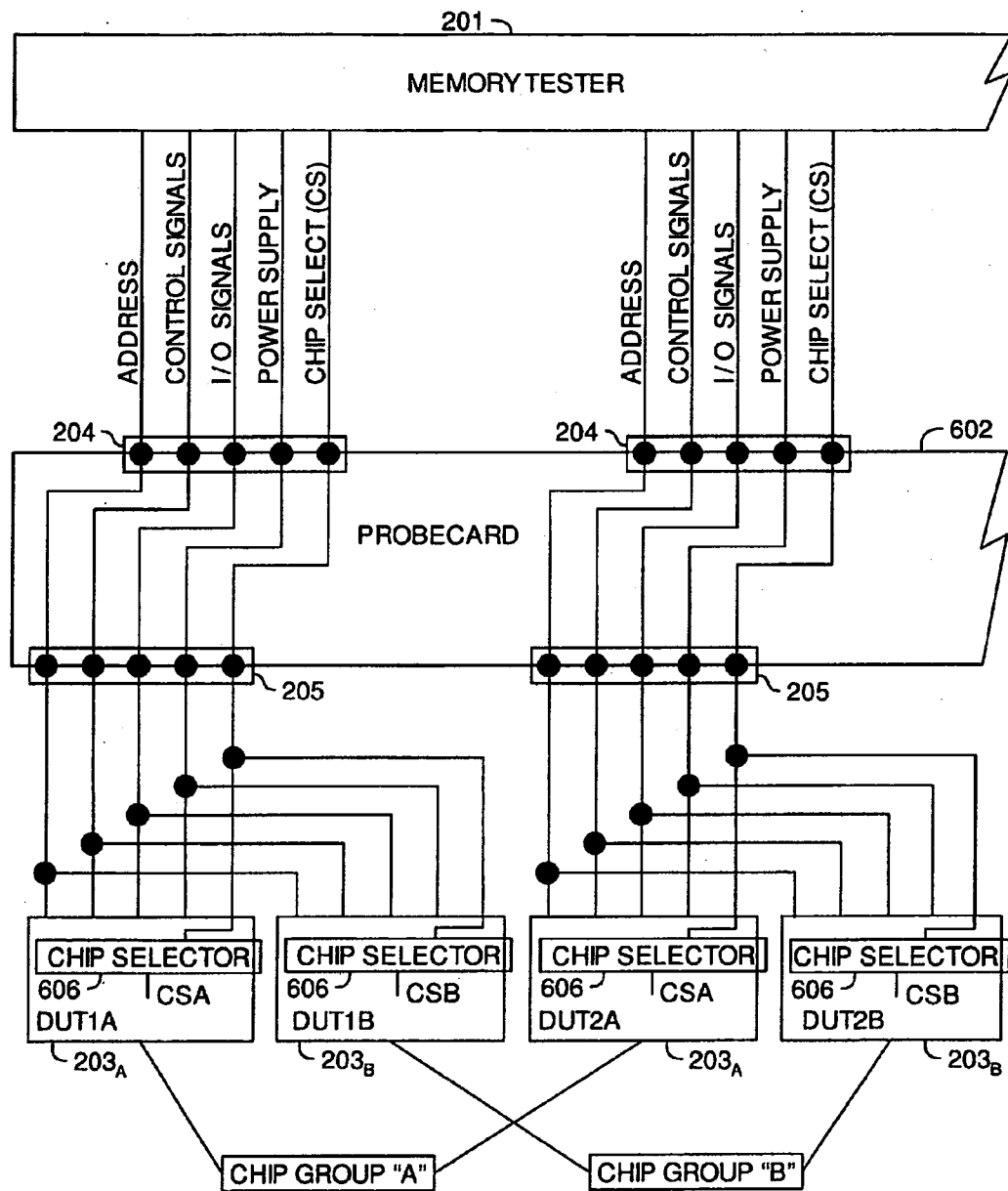


FIG. 6A

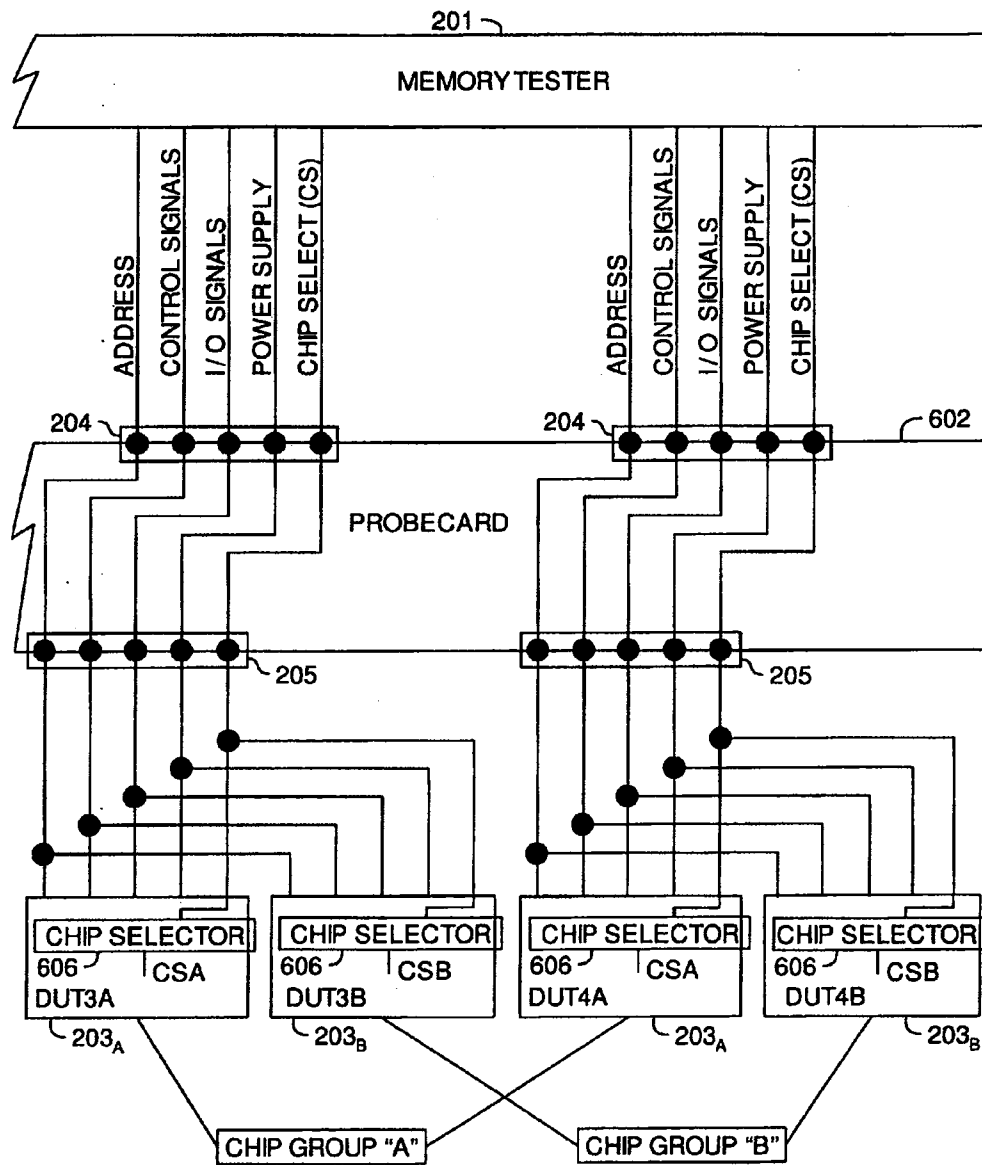


FIG. 6B

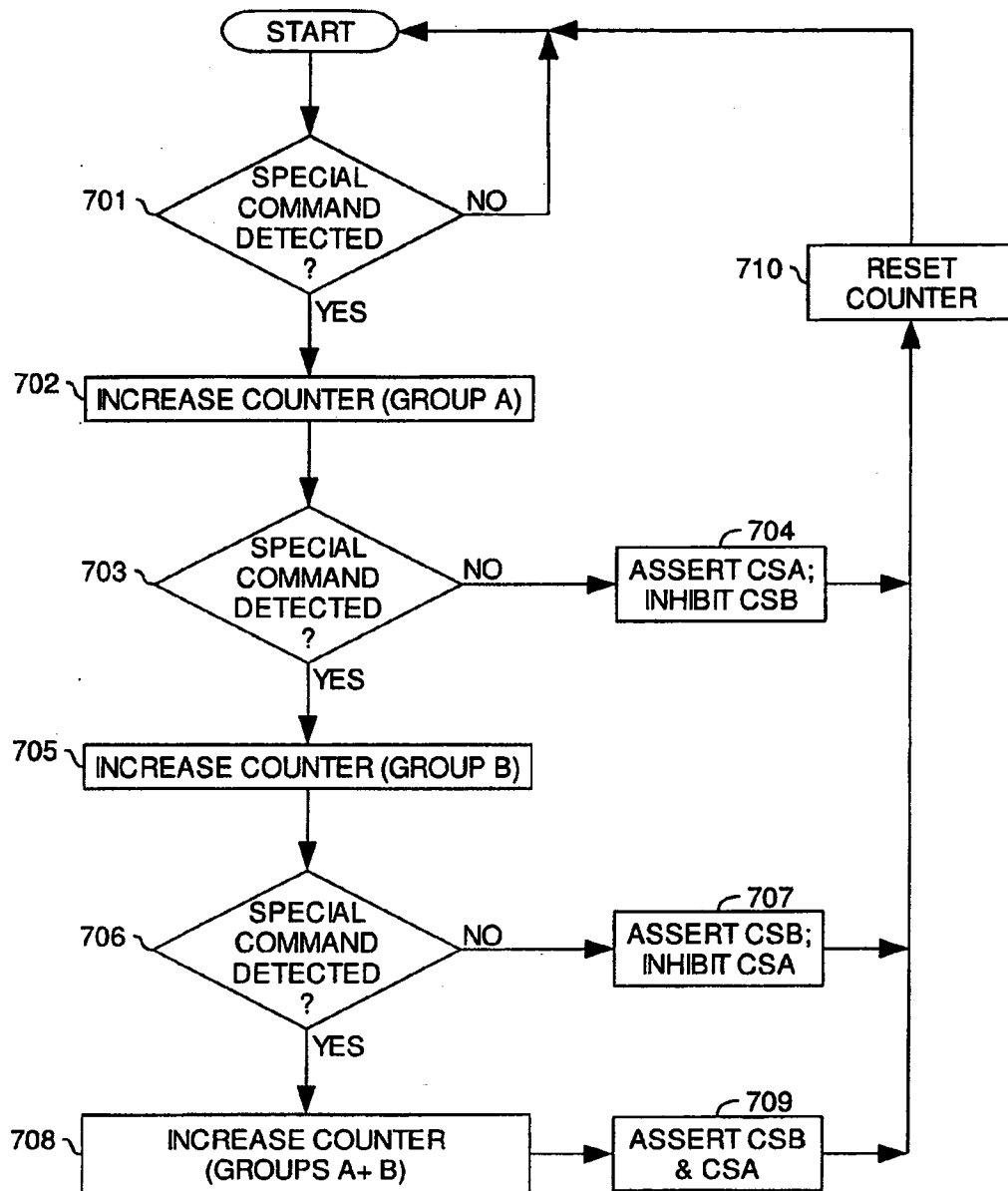


FIG. 7

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TEST PARALLELISM INCREASE BY TESTER CONTROLLABLE SWITCHING OF CHIP SELECT GROUPS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention generally relates to testing a plurality of memory devices in parallel and more specifically to increasing the level of parallelism in testing the memory devices.

[0003] 2. Description of the Related Art

[0004] Testing is a critical step in the production of memory devices. Testing allows for defective products to be identified, repaired or removed from the supply chain, thereby ensuring that only the best quality products are delivered to customers. Testing may also expose design flaws and provide useful yield information which, when fed back into the fabrication process, can improve quality and efficiency of production. Therefore, it is highly desirable to perform testing and to acquire testing data at the earliest possible time.

[0005] Memory testing may comprise providing address signals, control signals for commands, power supply, and input/output (I/O) signals. Testing, for example, may involve performing a write operation. The write operation may be performed by first selecting an address location for the write operation by asserting the address along the address lines. The data to be written may then be provided along the data lines to write the data in the selected address location. Thereafter, a read operation may be performed at the address where the write was performed to verify that the data retrieved is indeed the data that was written. To perform the read operation, the address may be asserted again along the address lines and the data on the data lines may be captured. The control signals may be used to indicate the type of command being executed to facilitate communication between devices.

[0006] One solution to reducing total testing time and improving throughput is to simultaneously test multiple memory devices in parallel. FIG. 1 illustrates an exemplary parallel testing system 100. The system consists of a memory tester 101, a probe card 102 and one or more devices under test (DUT) 103. Dedicated lines flow from the memory tester 101 to the DUTs 103 through the probe card 102. As illustrated, sets of address, control, I/O, power and chip select lines flow from the memory tester 101 to a respective set of input ports 104 on probe card 102. Each set of input ports 104 is communicable coupled with a set of output ports 105. Each of output ports 105 is coupled with a respective DUT 103. With multiple address, control, I/O, power and chip select lines being provided, multiple devices may be tested in parallel. For example, in system 100 up to four devices may be simultaneously tested, thereby reducing testing time by a factor of four.

[0007] However, the increasing density and complexity, of modern memory devices has meant longer test times per device and lower test throughput rates. Combating the increasing testing times has typically involved increasing the number of devices being tested in parallel. However, increasing the number of devices tested in parallel has meant

increased pin counts and complexity of memory testers and probe cards. This in turn results in increased testing costs.

[0008] Therefore, what is needed are systems and methods for increasing the level of parallelism in memory testing in a more efficient manner.

SUMMARY OF THE INVENTION

[0009] Embodiments of the invention generally provide methods and systems for increasing the level of parallelism in testing memory devices. A set of test signals provided by a memory tester may be shared by two or more devices under test. A chip selector may be used to select at least one or all the devices sharing a given set of test signals. By sharing test signals between multiple devices, the level of parallel testing may be increased without increasing the pin count and complexity of memory testers and probe cards.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0011] FIG. 1 is an illustration of a parallel memory test system according to the prior art.

[0012] FIG. 2 is an illustration of an exemplary test system according to one embodiment of the invention.

[0013] FIG. 3 is a flow diagram of exemplary operations performed to select one or more memory devices connected in parallel.

[0014] FIG. 4 is a flow diagram of an exemplary test plan.

[0015] FIG. 5 is a flow diagram of operations that may be performed by a chip selector to select one or more memory devices to which it is coupled.

[0016] FIG. 6 is an illustration of an exemplary test system according to another embodiment of the invention.

[0017] FIG. 7 is a flow diagram of operations that may be performed by a chip selector contained in a memory device to select or deselect the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0018] Embodiments of the invention generally provide methods and systems for increasing the level of parallelism in testing memory devices. A set of test signals provided by a memory tester may be shared by two or more devices under test. A chip selector may be used to select at least one or all the devices sharing a given set of test signals. By sharing test signals between multiple devices, the level of parallel testing may be increased without increasing the pin count and complexity of memory testers and probe cards.

[0019] In the following, reference is made to embodiments of the invention. However, it should be understood that the invention is not limited to specific described embodiments.

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Instead, any combination of the following features and elements, whether related to different embodiments or not, is contemplated to implement and practice the invention. Furthermore, in various embodiments the invention provides numerous advantages over the prior art. However, although embodiments of the invention may achieve advantages over other possible solutions and/or over the prior art, whether or not a particular advantage is achieved by a given embodiment is not limiting of the invention. Thus, the following aspects, features, embodiments and advantages are merely illustrative and are not considered elements or limitations of the appended claims except where explicitly recited in a claim(s). Likewise, reference to "the invention" shall not be construed as a generalization of any inventive subject matter disclosed herein and shall not be considered to be an element or limitation of the appended claims except where explicitly recited in a claim(s).

SPECIAL PROBE CARD CONFIGURATION

[0020] FIG. 2 illustrates an exemplary test system 200 according to one embodiment of the invention. System 200 comprises a memory tester 201, probe card 202 and a plurality of DUT's 203. A plurality of sets of test signals 106 couple the memory tester 201 to a respective set of input ports 204 of probe card 202, as illustrated. Four such input ports 204 are shown. Each set of input ports may comprise ports to receive address, control, I/O, power and chip select signals. While address, control, I/O, power and chip select signal ports are illustrated, one skilled in the art will recognize that any combination of the above mentioned signals or any additional signal ports may be utilized for performing the necessary testing operations.

[0021] Each set of input ports 204 may be communicably coupled with a respective set of output ports 205, as illustrated. Each set of output ports 205 may be coupled with two or more devices under test 203. Therefore, the test signals received from the memory tester through a set of input ports 204 may be shared by the two or more DUTs 203 connected to a respective set of output ports 205. Note however, that in the particular embodiment illustrated in FIG. 2, the chip select signal is not shared between parallel devices. While two DUTs 203 are shown connected to each set of output ports 205, one skilled in the art will recognize that any number of DUTs may be connected to each set of output ports 205. The greater the number of devices connected to each output port, the greater may be the level of parallelism achieved. Moreover, the increase in parallelism may be achieved without significant increases in the complexity and pin count of the memory tester or the probe card.

[0022] The number of DUTs connected in parallel, for example, may depend on the available power supply. The greater the number of DUTs connected to each set of output ports, the greater may be the need for power to drive all the connected DUTs. Therefore, the selection of the number of DUTs connected in parallel may depend on the availability and cost of power supply to the parallel devices. The number of DUTs connected in parallel may also depend on the size, density and the complexity of the DUTs and the Address Fail Memory available on the memory tester. For example, the address fail memory must be sufficient to record failures of the numerous DUTs connected in parallel. Large, dense and/or complex DUTs may require more address fail memory because the likelihood of failure may be greater.

[0023] A chip selector 206 may be associated with each pair of input ports sets 204 and output ports sets 205. The chip selector 206 may receive as an input the chip select signal received from the memory tester 201 in a respective input port in the set of input ports 204. Similarly, the chip select port may also receive as an input the control signals sent by the memory tester. Furthermore, the chip selector may drive device chip select lines connecting the chip selector 206 to each DUT through an associated set of output ports 205. Accordingly, device chip select lines CSa and CSb from the chip selectors to respective devices 203a and 203b are shown in FIG. 2. The number of chip select lines may, for example, depend on the maximum number of DUTs that may be connected to a set of output ports 205.

[0024] FIG. 3 illustrates a flow diagram of exemplary operations that may be performed by a chip selector to select one or more devices connected to a set of output ports 205. The operations begin in step 301 by receiving the chip select signal from the memory tester 201. In step 302 the chip selector may determine the specific DUTs to be selected for testing. In one embodiment the chip selector may monitor the command signals sent by the memory tester to determine the specific DUTs to be selected. The programming of the chip selector is described in greater detail below. In response to determining the specific DUTs to be selected, the chip selector may assert the device chip select signals, CSa and CSb for example, to activate the DUTs for testing.

[0025] FIG. 4 is a flow diagram of steps to perform the previously described memory test operations on the DUTs illustrated in FIG. 2. As described earlier the memory test operations may constitute performing a write operation at an address location followed by a read operation at that address location to ensure that the data written is indeed the data retrieved from the read operation. One advantage of the invention is that all DUTs connected to the probe card may be selected at once and a write operation may be performed on all the DUTs in parallel. Therefore, the operations may begin in step 401 by selecting all the DUTs. The memory tester may, for example, assert the chip select signal to each chip selector. Thereafter, the memory tester may assert the appropriate command signals to the chip selectors to indicate that all DUT's connected to the respective set of output ports must be selected. The chip selectors may assert the respective device chip select signals (CSa and CSb for example) in response to the command signals.

[0026] In step 402, the memory tester may perform a write operation by asserting data along the data lines of each set of input ports 204. This data may be written to the DUTs through each of the sets of output ports 205.

[0027] While it is desirable to perform the write operation in parallel across all devices, the read operation may be performed only on select devices. The read operation may be performed in this manner to facilitate identification of specific devices that are defective. The selection of specific devices may be accomplished by selecting, while reading, specific devices connected to each set of output ports rather than selecting all devices connected in parallel. Accordingly, in step 403, the memory tester may assert the chip select signal to the chip selector and issue commands indicating that only chip group a be selected. In response the chip selector may assert only the CSa signals to activate DUTs 203a.

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[0028] A read operation may then be performed on DUTs 203a in step 404. In step 405, the read data may be compared to the write data to verify proper functioning of the memory device. In step 406, if the read data is not the same as the data written, a failure may be recorded in the address fail memory of the memory tester identifying the failing DUT. A memory tester may similarly perform a read operation on chip group b by asserting the chip select signal and issuing commands to the chip selectors to select chip group b. Information about failing devices in chip group b may also be recorded in the memory tester. Furthermore, the steps described above may be repeated for various address locations of the DUT.

[0029] While a sequence of read and write operation is described herein, one skilled in the art will recognize that any sequence read and write operations may be performed while testing. Moreover, several other types of tests may be run on the device. For example, the DUTs may be subject to a stress test to test the durability of the devices. The selection of specific DUTs under test may be made appropriately according to the particular test plan being implemented.

[0030] FIG. 5 is a flow diagram of the programming of a chip selector according to one embodiment of the invention wherein the chip selector determines the devices to be selected based on a sequence of command signals received. The operations begin in step 501 with the chip selector detecting a special command. Upon receipt of the special command, the chip selector may increase a counter maintained by the chip selector. At the first increment of the counter, in step 502, the chip selector may select chip group a. In step 503, if no further special command is detected, the chip selector is set to chip group a. The CSa signal may be asserted and the counter may be reset in step 504. If, on the other hand, a further special command is detected, the counter may be further increased in step 505. If the further special command is not detected in step 506, the chip selector is set to chip group b. The CSb signal may be asserted and the counter may be reset in step 507. If, on the other hand, yet another special command is detected, the counter is further increased and the chip selector may be set to chip groups a and b in step 508. In step 509 the counter may be reset and both CSa and CSb signals asserted to select all DUTs.

[0031] As illustrated in FIG. 2, the control signals asserted by the memory tester may be received by both the chip selectors and the DUTs. Therefore, the special command selected may be such that it may only be comprehended by the chip selectors. Because the special command is not understood by the DUTs there is no reaction in the DUTs upon receipt of the special commands.

[0032] One skilled in the art will also recognize that an advantage of the present invention is that several different types of memory devices may be tested in parallel. This may be especially useful to manufacturers producing a wide variety of memory products tailored to different customer requirements. The present invention does not require a focused test platform to test memory devices thereby increasing the flexibility and reusability of the test system for diverse product lines. For example, a manufacturer may be able to test a DRAM or flash device along with test wafers simultaneously within the same test system as long as they fall within the operable ranges of memory.

SPECIAL CHIP DESIGN CONFIGURATION

[0033] FIG. 6 illustrates an exemplary test system 600 according to another embodiment of the invention. As in system 200, system 600 also contains a memory tester 201, a probe card 602 and a plurality of DUTs 203. Probe card 602, unlike probe card 202, does not contain any chip selectors. Instead the chip selector circuitry is fused on to each of the DUTs, as illustrated in FIG. 6. Therefore, in this embodiment the chip select signal sent by the memory tester is shared between the parallel devices and is routed directly to the DUTs through the probe card 602. The chip select signal is received by the chip selectors contained in the individual DUTs. The chip selector in a particular DUT determines whether the DUT is selected for testing based on the chip select signal, the command signals and on the chip group to which it belongs. The chip groups may be pre-defined in a wafer prior to testing to facilitate the identification of test modes.

[0034] FIG. 7 is a flow diagram of the programming of a chip selector from FIG. 6 according to one embodiment of the invention wherein the chip selector determines whether a respective device is selected based on a sequence of command signals received. The operations begin in step 701 with the chip selector detecting a special command. Upon receipt of the special command, the chip selector may increase a counter maintained by the chip selector. At the first increment of the counter, in step 702, the chip selector may select chip group a. In step 703, if no further special command is detected, and the chip selector is associated with a DUT in group a, CSa is asserted and the device is activated. On the other hand, if the chip selector is associated with a device in group b, CSb is inhibited and the device is not activated. The counter is then reset in step 710.

[0035] If, on the other hand, a further special command is detected, the counter may be further increased in step 705. If yet another special command is not detected in step 706, and the chip selector is associated with a DUT in group b, CSb is asserted and the device is activated. On the other hand, if the chip selector is associated with a device in group a, CSa is inhibited and the device is not activated. The counter is then reset in step 710.

[0036] If, on the other hand, yet another special command is detected, the counter is further increased and the chip selector may assert the device chip select signal. In this instance the device chip select signal CSa and CSb are both asserted and the grouping of the device may be irrelevant. The counter is then reset in step 710.

CONCLUSION

[0037] By allowing two or more DUTs to share the same test signals, embodiments of the present invention increase the level of parallelism in testing memory devices and reduce testing time. Furthermore, the increase in parallelism is achieved without significant increases in pin counts or complexity of memory testers and probe cards.

[0038] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

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What is claimed is:

1. A system for testing a plurality of memory devices, comprising:

a) a probe card comprising:

a plurality of sets of input ports, each set of input ports comprising:

at least two input ports each configured to receive a respective test signal; and

a chip select port configured to receive a chip select signal;

a plurality of sets of output ports each communicatively coupled to a respective one of the sets of input ports; each set of output ports comprising:

at least two output ports communicatively coupled to a respective one of the at least two input ports of the respective set of the input ports; and

b) a separate chip selector for each set of input ports and respective set of output ports, wherein each chip selector is configured to:

receive the chip select signal from the respective chip select port;

receive a command signal via one of the input ports of the respective set of input ports, wherein the command signal is one of the test signals; and

in response to the received command signal, issue at least one chip selection signal to select, for testing, at least one of two or more memory devices connected to the set of output ports.

2. The system of claim 1, wherein the chip selection signal is configured to activate the memory device for testing.

3. The system of claim 1, wherein the chip selectors are contained in the probe card, and wherein each chip selector is associated with each pair of the sets of input ports and sets of output ports.

4. The system of claim 1, wherein the chip selectors are configured to:

receive a succession of command signals; and

in response to receiving the succession of command signals, select one or more memory devices connected to the set of output ports based on the number of successive command signals received.

5. The system of claim 1, wherein the test signals comprise any combination of:

address signals;

data signals;

input/output signals; and

control signals.

6. A system for testing a plurality of memory devices, comprising:

a) a tester for issuing a plurality of test signals and a chip select signal;

b) a probe card, comprising:

a plurality of port sets, each set comprising:

a plurality of input ports each for receiving a respective test signal of the plurality of test signals; wherein one of the plurality of input ports is a command signal port for receiving a command signal;

a plurality of output ports each communicatively coupled to a respective input port; wherein each port set is communicatively coupled to N memory devices of the plurality of memory devices in parallel, where $N > 1$; and

a chip select port for receiving the chip select signal;

c) a separate chip selector for each port set for:

receiving the respective chip select signal from the respective chip select port;

receiving the respective command signal via the respective command signal port of the port set, wherein the command signal is one of the test signals; and

in response to the receiving the command signal, issuing the chip selection signal to select, for testing, one of the N memory devices connected to the output ports of the respective port set;

wherein the tester is further utilized for altering the command signal to simultaneously select different groups of the plurality of memory devices in order to test the memory devices of each group in parallel, each group comprising one of the N memory devices connected to the respective output ports of the respective port set.

7. The system of claim 6, wherein the chip selectors are contained in the probe card, and wherein each chip selector is associated with each pair of the sets of input ports and sets of output ports.

8. The system of claim 6, wherein the chip selectors are further provided for:

receiving a succession of command signals; and

in response to receiving the succession of command signals, selecting one or more memory devices connected to the set of output ports based on the number of successive command signals received.

9. A system for testing a plurality of memory devices, comprising:

a) a probe card comprising:

a plurality of sets of input ports, each set of input ports comprising:

at least two input ports each configured to receive a respective test signal;

a plurality of sets of output ports each communicatively coupled to a respective one of the sets of input ports; each set of output ports comprising:

at least two output ports communicatively coupled to a respective one of the at least two input ports of the respective set of the input ports; and

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- b) a separate chip selector for each set of input ports and respective set of output ports, wherein each chip selector is configured to:
- receive a command signal via one of the input ports of the respective set of input ports; and
 - on the basis of the command signal, selecting a specified memory device; the specified memory device being communicatively connected to one of the output ports.
10. The system of claim 9, wherein each chip selector is further configured to:
- decode the command signal to determine whether the decoded command signal specifies a selection of a memory device to test; and
 - if the decoded command signal specifies a selection of a memory device to test; selecting the specified memory device.
11. A method for testing a plurality of memory devices comprising:
- sending, by a memory tester, one or more test signals and a chip select signal to each of one or more sets of input ports of a probe card;
 - connecting two or more of the plurality of memory devices to each of one or more sets of output ports of a probe card, wherein the set of output ports is configured to assert the one or more test signals and at least one chip selection signal;
 - receiving by a plurality of chip selectors the chip select signal and a command signal, wherein the command signal is one of the test signals;
 - in response to receiving the chip select signal and the command signal, asserting, by the chip selector, the at least one chip selection signal to activate at least one of the two or more memory devices connected to the set of output ports; and
 - asserting the one or more test signals to test the at least one selected memory device.
12. The method of claim 11, further comprising:
- receiving, by the chip selector, a succession of command signals; and
 - asserting the at least one chip selection signal based on the number of successive command signals received.
13. The method of claim 11, wherein the plurality of chip selectors are contained in the probe card, and wherein each chip selector is associated with each set of output ports of the probe card.
14. The method of claim 11, wherein each of the plurality of chip selectors is contained in each of the plurality of memory devices.
15. The method of claim 14, wherein the chip select signal is the chip selection signal.
16. The method claim 11, wherein the test signals comprise any combination of:
- address signals;
 - data signals;
 - Input/Output signals; and
 - Control signals.
17. A system for testing memory devices, comprising:
- a) a plurality of memory devices;
 - b) a probe card, comprising:
 - a plurality of port sets, each set comprising:
 - a plurality of input ports each configured to receive a respective test signal of a plurality of test signals issued by a tester;
 - wherein one of the plurality of input ports is a command signal port configured to receive a command signal;
 - a plurality of output ports each communicatively coupled to a respective input port; wherein each port set is communicatively coupled to N memory devices of the plurality of memory devices in parallel, where $N > 1$; and
 - a chip select port configured to receive a chip select signal from the tester;
 - c) a separate chip selector resident on each memory device, wherein the chip selectors associated with a given port set are configured to:
 - receive the same chip select signal from the respective chip select port;
 - receive the same command signal via the respective command signal port of the port set; and
 - in response to the received command signal, select or deselect, for testing, the respective memory device on which the respective chip selector resides; wherein only one of the N memory devices of the given port set is selected for testing at a given time.
18. The system of claim 17, wherein in response to receiving the command signal the chip selector is further configured to assert a chip selection signal, wherein the chip selection signal is configured to activate or deactivate the memory device for testing.
19. The system of claim 17, wherein the chip selectors are configured to:
- receive a succession of command signals; and
 - in response to receiving the succession of command signals, select or deselect the memory device.
20. The system of claim 17, wherein the test signals comprise any combination of:
- address signals;
 - data signals;
 - input/output signals; and
 - control signals.
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